Junction field-effect-transistor-based germanium photodetector on silicon-on-insulator

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We propose and demonstrate a novel Ge photodetector on silicon-on-insulator based on a junction field effect transistor structure, where the field-effect transistor gate is replaced by a Ge island with no contact on it. Light incident on the Ge switches on the device by altering the conductance of the Si channel through secondary photoconductivity. The device's sensitivity is also enhanced by a vast reduction in parasitic capacitance. In cw measurements, proof-of-concept detectors exhibit up to a 33% change in Si channel conductance by absorbing only 200 nW of power at 1.55 μm. In addition, pulsed response tests have shown that rise times as low as 40 ps can be achieved. © 2008 Optical Society of America

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The recent interest in Si photonics [1] has sparked many advances in the design and fabrication of various optical components on a complementary metal-oxide semiconductor (CMOS) platform including modulators, photodetectors, and lasers. To make photodetectors for high-speed transceivers at 1.55 μm, Ge epitaxial films have been successfully integrated with Si to fabricate highly efficient devices [2,3]. These detectors show very good responsivity combined with bandwidths suitable for 10 Gbits/s applications. However, in spite of their excellent characteristics, there are limits to the extent to which they can be miniaturized relative to conventional CMOS devices. In the context of optical integration, a photodetector based on a field-effect transistor (FET) structure would represent a highly practical and scalable optoelectronic component. In this Letter we propose and give proof-of-concept demonstrations of such a Ge photodetector based on a transistor design that utilizes secondary photoconductivity [4].

The design of the device is based on an FET, where the gate is replaced by a Ge island on the Si channel but where no contact is made to the Ge [Fig. 1]. Infrared light is incident on this island either at normal incidence or through a waveguide. Owing to the large valence band discontinuity at the p-Ge/n-Si interface [5] (inset of Fig. 1), the photohole collection is highly suppressed, and the diffusion of photoelectrons from the Ge into the Si is the dominant photoresponse mechanism. As the Ge–Si heterojunction is an open circuit, this gives rise to an excess positive charge in the Ge, which in turn attracts electrons in the Si channel underneath, thereby modulating its conductance. The operation is therefore that of a junction-field-effect-transistor (junction-FET). The photoelectron current flowing across the open Ge–Si junction creates forward bias to achieve zero net current, and this bias is the gate voltage that changes the Si depletion and opens up the channel. Since the trapped holes continue to affect the channel current until they become neutralized, the device can show a large amount of gain depending on the dielectric relaxation time of the holes (τ_R) and its magnitude relative to the channel transit time of the electrons.

Besides its inherent gain mechanism, the great advantage of the device lies in the unique scaling opportunities that it presents since the Ge gate length could easily be reduced to state of the art metal-oxide semiconductor field-effect transistor (MOSFET) dimensions. The reduction in Ge-island capacitance

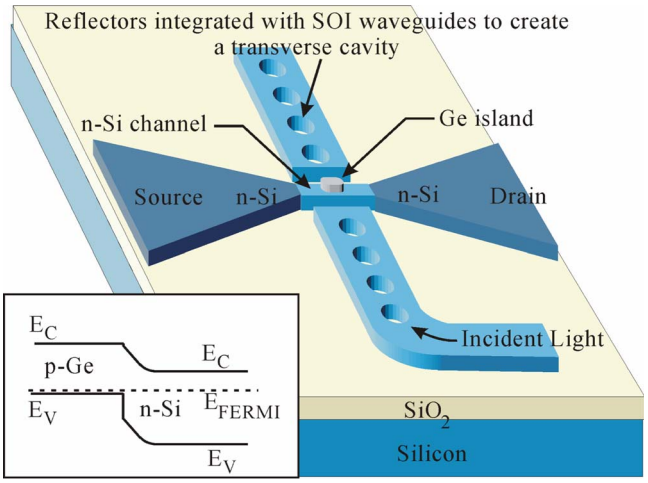

Fig. 1. (Color online) Schematic of a "photoheterojunction FET." A Ge island deposited on the channel of an FET acts as a gate. When photocarriers are created in the Ge, the band alignment at the interface (see inset) facilitates the trapping of photoholes in the Ge. The resultant charge separation modulates the Si channel conductance and therefore emulates junction-FET behavior.

that would accompany the scaling would greatly improve the performance of a receiver that employs the device [6]. If the capacitance is small enough, a very small amount of photocharge produced by the detector will be sufficient to produce a large enough voltage swing to switch the device. Therefore, as the gate area is lowered, the sensitivity of the detector proportionately increases. Furthermore, the absence of contacts on the Ge island also eliminates any stray capacitance. The lower optical absorption cross section of a smaller Ge gate can be countered by embedding the detector in an optical cavity (as shown in Fig. 1). There is potential, therefore, to fabricate significantly miniaturized detectors that exhibit very high responsivity.

Proof-of-concept detectors (Fig. 2) based on the above design were made as follows: Initially, 200 nm thick p-Ge films were directly deposited onto n-silicon-on-insulator wafers using molecular beam epitaxy at 370°C following a high temperature anneal to clean the surface [7]. The low temperature growth makes the fabrication compatible with a back-end process [8], although front-end Ge processing has also started gaining wide acceptance in CMOS foundries. The disadvantage of the growth at 370°C is that the resulting Ge films are heavily dislocated and have low effective photoelectron collection lengths [9]. After the Ge epitaxy, the detectors were fabricated using electron-beam lithography and reactive ion etching (Cl_2+BCl_3 for Si and CH_4 for Ge). The Si channel was always designed as a square with the Ge gate completely covering it, although in some of the smaller devices the final W/L ratio was <1 owing to fabrication inconsistencies. As indicated in Fig. 2(a) the channel length was varied between $\sim$1 and 4 μm. Electron-beam lithography enabled us to align the Ge island within 50 nm of the Si channel, thereby maximizing detector sensitivity. To minimize parasitic series resistance, self-aligned ohmic contacts to the Si were made by high-dose (2×10^{15} cm^{-2}, 35 keV) phosphorus implantation using the same mask as the one used to pattern the Ge gate. Since Ge melts at 940°C and significant intermixing between the Ge and Si can occur at much lower temperatures, typical source-drain activation anneals were avoided in our process flow because they utilize temperatures well in excess of 900°C. Instead, to ensure that the Ge was not damaged during the anneal, low-temperature solid phase epitaxy [10] at 650°C was used to activate the dopants. After the activation, Ti–Al contacts to the Si were made using thermal evaporation. Figure 2(b) shows a scanning electron microscope (SEM) picture of a finished 4 μm device.

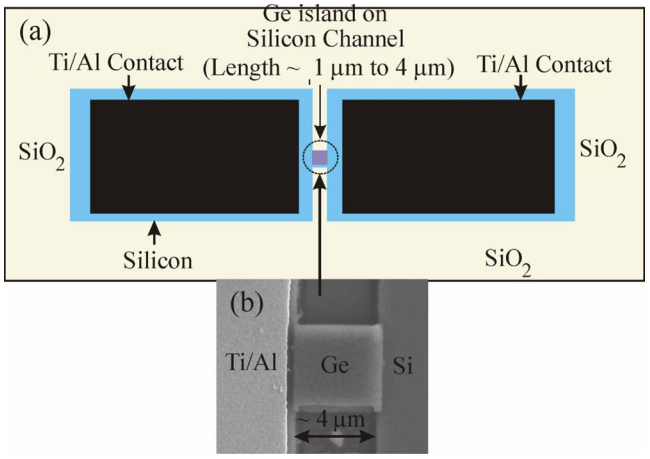

Fig. 2. (Color online) (a) Top view of the fabricated devices. (b) Zoomed-in SEM picture of the channel.

The experiments were done with cw and pulsed light at 1.55 μm, which was normally incident on the devices and focused down to a 10 μm spot with a high NA objective. The source-drain bias (V_{SD}) was applied through a bias-tee, and the high-speed signal was recorded with a 20 GHz sampling oscilloscope with extensive averaging done to improve signal-to-noise. In the regime before the device enters deep saturation, an increase in V_{SD} would give higher photoresponse, since any change in conductance would result in a relatively larger change in the channel current. However, the improved responsivity would also be accompanied by an increase in dark current and power dissipation. As these devices are intended to be used in highly integrated intrachip applications, where the power consumption can be critically important, their characterization was done with the source-drain bias limited to 0.5 V.

Figure 3 shows the results of the cw experiments. The percentage increase in channel conductance is plotted against the optical power absorbed at 1.55 μm for devices with two different gate sizes (since the gates are much smaller than the beam spot and the Ge film is only 200 nm thick, the amount of light absorbed is very low). Ramping up the incident power is equivalent to raising the gate's forward voltage, and the resultant saturation of the increase in conductance can clearly be seen. As expected, the plot also shows that the sensitivity of the smaller device is higher and that the amount of light needed to pro-

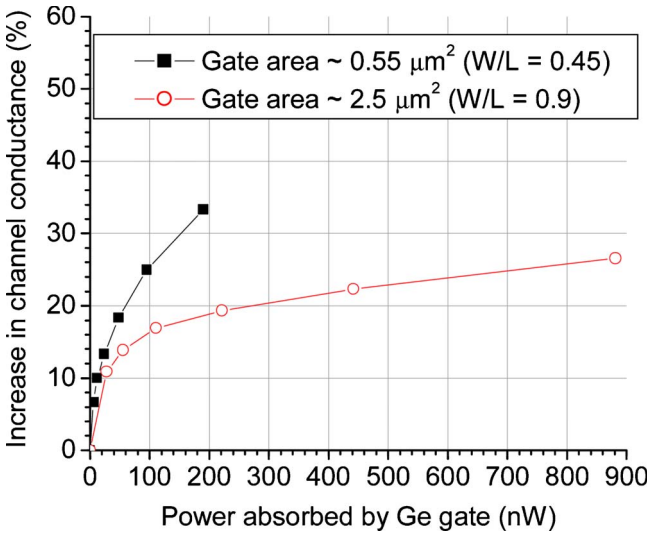

Fig. 3. (Color online) Percentage increase in channel conductance versus power absorbed by the Ge gate at 1.55 μm (0.5 V source-drain bias). The effect of the light saturates, which is analogous to the effect of the gate voltage on the characteristics of a normal FET. The smaller device shows higher sensitivity.

duce a certain change in channel conductance is roughly proportional to the gate area. In the case of the 0.55 μm^2 detector, the absorbed power is of the order of 200 nW for a 1 mW input beam, and that amount of light changes the channel conductance from 6×10^{-6} to $8\times10^{-6}\,\Omega^{-1}$. As the bias was 0.5 V, this translates into a channel current change of $\sim1\,\mu A$. Hence the cw responsivity of the device is ~5 A/W, which demonstrates the large photoconductive gain that can be extracted from this configuration. For purposes of comparison, the nominal responsivity of a standard surface illuminated p-Ge/n-Si detector with a similar Ge quality would be a few milliampere per watt [9].

To look at the pulsed response of the detectors, we used 1 ps mode-locked pulses at 1.55 μm (1 mW average power, 20 MHz repetition rate). The results for the 2.5 μm^2 device are plotted in Fig. 4. The peak output is of the order of only a few 100 μV because it is obtained across a 50 Ω load. It can be seen that rise times as short as ~40 ps are observed (inset of Fig. 4), which is very promising for high-speed applications. The magnitude of the pulsed response and the rise time are in reasonable agreement with values predicted by conventional FET models [11]. It is also evident from Fig. 4 that the main caveat of these detectors is the fall time (τ_F), which is of the order of tens of nanoseconds. The fall time here is the RC time constant for the depletion capacitance at the Ge–Si junction since the charge-separation created by the diffusion of the photoelectrons charges the depletion capacitance that then has to discharge through the forward resistance of the diode. Therefore $\tau_F=R_FC_G=(\eta V_{th}/I_F)C_G$, where C_G is the gate capacitance, η is the diode quality factor, V_{th} is the thermal voltage, and I_F is the forward current (which provides the electrons needed to recombine with the trapped holes in the Ge). For the device in question τ_F is estimated to be ~250 nS. The measured value is ~40 nS, which may be due to additional charge leakage mechanisms at the edge of the Ge mesa.

The long tail recorded in the pulsed response is not unexpected, since this is a problem typical of devices based on trapped charges. Fortunately, the slow fall times can be countered by device designs that increase the leakage current at the p-Ge/n-Si junction so as to facilitate the recombination of the trapped photoholes. Since a higher bandwidth will be accompanied by lower gain, the detector design should optimize τ_F so that a suitable trade-off between sensitivity and speed can be achieved.

In conclusion, we have proposed and demonstrated a novel Ge–Si photodetector based on a junction-FET structure that exhibits low rise times and high sensitivity. It is especially suitable for intrachip applications because the low capacitance of the detector enables it to produce large output voltages at extremely small photocurrent levels. The unique scalability of the device and its compatibility with conventional CMOS chips makes it very attractive for use in an integrated optoelectronic platform.

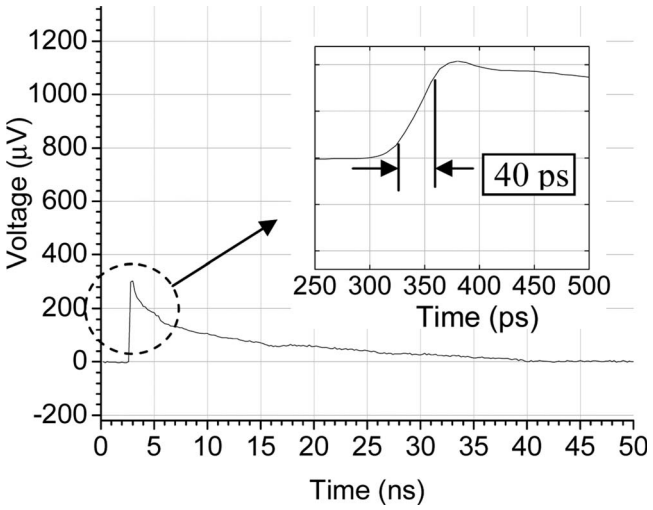

Fig. 4. Response to a 1 ps mode-locked pulse with the rise time in the inset (0.5 V source-drain bias).

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