Sputtered gold as an effective Schottky gate for strained Si/SiGe nanostructures

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Metallization of Schottky surface gates by sputtering Au on strained Si/SiGe heterojunctions enables the depletion of the two dimensional electron gas at a relatively small voltage while maintaining an extremely low level of leakage current. A fabrication process has been developed to enable the formation of submicron Au electrodes sputtered onto Si/SiGe without the need of a wetting layer. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2430935]

Significant effort has been directed toward the development of electrostatically defined quantum dots as potential elements for quantum computation information. While a high level of control and sophistication has been achieved in current GaAs/AlGaAs based structures,[1] silicon based heterostructures are expected to have the distinct advantage of possessing extremely long electron phase coherence lifetimes,[2,3] which can be attributed to the small spin-orbit interaction and the low natural abundance of isotopes with nuclear spin.

Means of control in lateral quantum dot devices is often exercised through the use of Schottky barrier top gates in which metal electrodes patterned on the semiconductor surface capacitively couple to the two dimensional electron gas (2DEG). By applying a bias on the gates one can selectively deplete the charge carriers in the 2DEG directly below, and in the vicinity of, the gates, thereby controlling current flow. Over the last several years attempts were made to create mesoscopic devices on strained Si/SiGe heterostructures by directly mimicking the existing geometries and fabrication processes that have been employed on GaAs/AlGaAs based heterostructures. The success was often limited due to the high level of leakage current and/or the incomplete depletion of the 2DEG by Schottky gates on strained Si/SiGe. Several innovative approaches have recently been introduced as means of circumventing these obstacles.[4–6] These methods primarily focus on the formation of side gates through various etching techniques. Unfortunately, in order to reach a comparable level of stability, control, and effectiveness of confinement achieved in GaAs based structures, devices using multiple surface gates will most likely be required. Towards this end, both Berer *et al.*[7] and Slinker *et al.*[8] have used evaporated Pd on strained Si/SiGe as Schottky gates with positive results. Despite this encouraging development, it is recognized that further improvement of the effectiveness of the Schottky gates is needed to gain control in the few-electron regime.

In this letter, we demonstrate that significant improvements to Schottky gates on Si/SiGe can be made by the proper choice of gate metal and a simple change in the mechanism of gate metal deposition. In particular, we found that the Schottky gates formed by sputtering Au on strained Si/SiGe heterojunctions enable the depletion of the 2DEG at a relatively small voltage while maintaining an extremely low level of leakage current.

The devices used for our experiment were fabricated on modulation doped Si/SiGe heterostructures, which are commonly used for the fabrication of lateral quantum dots. These samples have a peak mobility of about 10^5 cm^2/V s at a density of 3×10^{11}/cm^2 and are grown by molecular beam epitaxy with a layer by layer composition as follows: Si(5 nm)/SiGe$_{0.25}$(35 nm)/δ-doped Sb=2 $\times10^{12}$ cm^{-2}/SiGe$_{0.25}$(22.5 nm)/Si(15 nm)/SiGe$_{0.25}$(1 μm)/SiGe$_{0.20-0.25}$(0.9 μm)/SiGe$_{0.108-0.20}$(1.5 μm)/SiGe$_{0.018-0.108}$ (1.5 μm)/Si(100 nm)/p-Si(100) substrate.

To test the effectiveness of various Schottky gates, a large square gate $(150\times150\ \mu\text{m}^2)$ was defined by UV lithography atop a chemically etched mesa. Ohmic contacts to the 2DEG were formed by phosphorous ion implantation. Pd, Cr, and Au films were deposited as gate metals by evaporation. The coupling strength between the gate and 2DEG (i.e., depletion voltage) as well as leakage between the gate and 2DEG were both measured as a function of applied voltage (Fig. 1). The results of the leakage current from the evaporated gates are in line with the known Schottky barrier values. For Pd the onset of measurable leakage began at a larger value of applied bias, in accordance with the larger Schottky barrier it forms with n-type silicon. However, in terms of effectiveness of gate coupling, Pd required a correspondingly larger value of bias to fully deplete the 2DEG. The strongest coupling between gate and 2DEG was found with Au, which required only a very small voltage for the complete depletion of the 2DEG, but had unacceptably high levels of leakage current. The widely varying voltages necessary to cause depletion cannot be corroborated by a simple Schottky barrier analysis.

The Schottky-Mott theory predicts that the Schottky barrier height, Φ_B, will depend linearly on the metal work function $\Phi_B=(\Phi_m-\chi_s)$, where Φ_m is the work function of the metal and χ_s is the electron affinity of the semiconductor. This relation does not always hold in practice. When a metal

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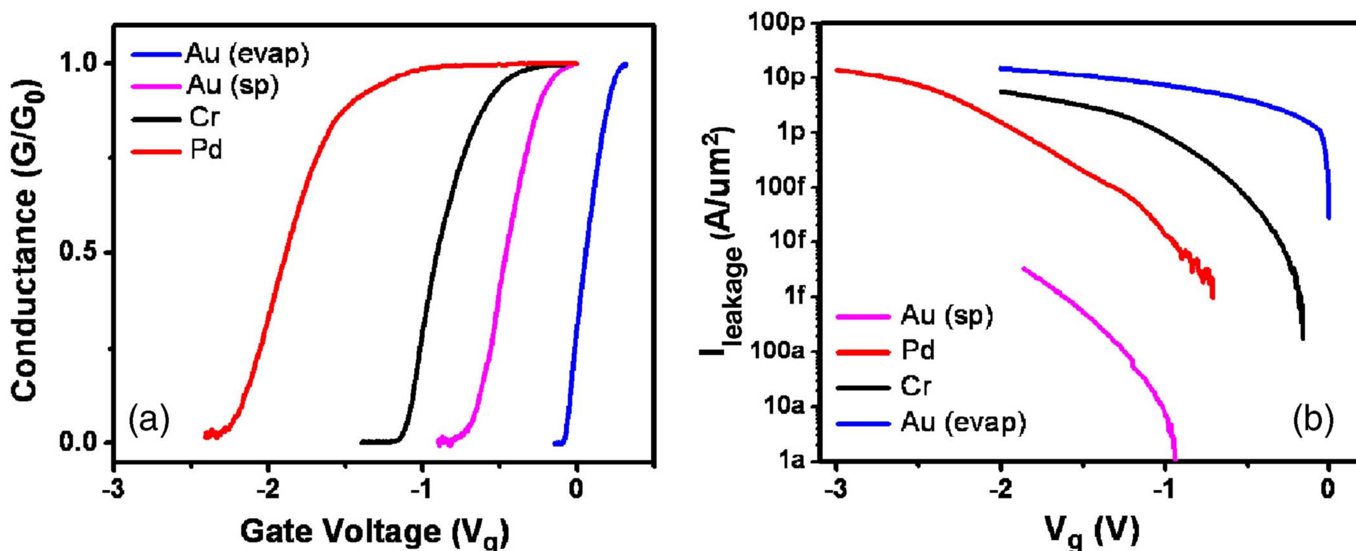

FIG. 1. (Color online) (a) Conductance measured as a function of applied gate voltage for four different gate compositions. (b) Leakage current per μm^2 of gate electrode measured as a function of applied voltage for the same four samples. Gates of sputtered Au demonstrate levels of leakage several orders of magnitude lower, on average, and possess strong coupling to the 2DEG.

and a semiconductor are joined together, Φ_B will depend sensitively not only on the identity of the materials but also on the details of the interface structure that results. In covalently bonded semiconductors, such as silicon, surface gates may be unable to effectively modulate the density of the underlying 2DEG due to localized surface charges. The large values of applied voltage necessary to cause depletion with Pd and Cr gates are indicative of correspondingly large surface charge densities.

The choice of gate metal will influence the relative magnitude of Φ_B, and a larger Φ_B dictates a lower level of leakage current from the metal to the semiconductor at a particular bias. But even though Pd, for example, has a relatively large Φ_B, a large voltage is also required to achieve depletion. Higher operating biases lead to increased levels of leakage current, which in turn compromise the surface gate characteristics.

We also deposited gold by sputtering instead of evaporation. Gates with a sputtered layer of gold always demonstrated dramatically less leakage current as compared to the evaporated gates, while maintaining excellent coupling to the 2DEG (Fig. 1). The kinetic energy of evaporated atoms corresponds to the temperature of the evaporating surface, and is therefore typically around 0.1–0.3 eV. The energy of sputtered atoms is roughly 100 times greater (for Au: ~8–16 eV).[9–11] According to the software program "Stopping and Range of Ions in Matter" (SRIM), sputtered gold atoms may penetrate into silicon to a depth of around 1 nm, while evaporated atoms will not penetrate at all. The ability of sputtered gold atoms to penetrate the silicon cap will promote an interdiffusion of gold and silicon, possibly triggering the formation of gold silicide compounds.[12,13] We speculate that, much akin to platinum silicide,[14] gold silicide may form a larger, more stable Schottky barrier with *n*-type silicon when compared to bare gold.

Unfortunately, thin films of Au will not customarily adhere well to silicon due to the SiO_2 that forms on the surface, causing serious problems during the lift-off phase of the fabrication procedure. By removing the native oxide layer with a buffered oxide etch (NH_3F:HF, 6:1), we found it possible to attain sufficient adhesion, enabling us to repeatedly and reproducibly form devices out of evaporated and sputtered Au without any lift-off problems.

Unlike the deposition of metal by evaporation, during the sputtering process metal is not deposited from one direction [Fig. 2(d)]. As argon ions bombard the sputtering target, gold atoms are deposited from many different directions. The result is that sputtering may generate complete coverage of the developed lithography pattern, making lift-off extremely difficult, if not impossible. This is especially problematic for thinner resists and finer lithographic structures, namely, for electron beam lithography using polymethyl methacrylate (PMMA) resist. Since the majority of nanoscale devices necessitate the use of electron beam lithography, a fabrication technique was required that would facilitate metallization by sputtering.

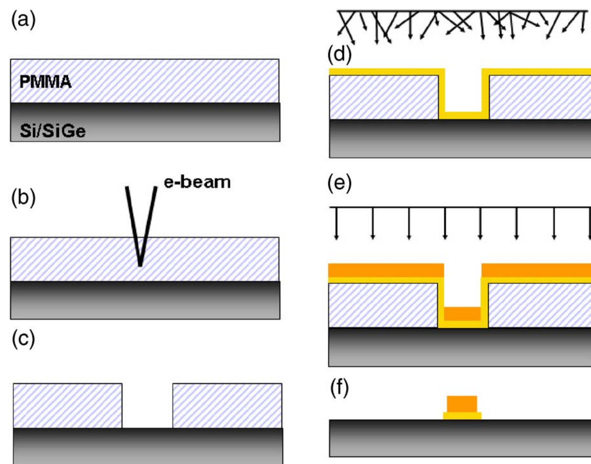

FIG. 2. (Color online) Fabrication steps. (a) The substrate is spin coated with 495 PMMA. (b) Electron beam lithography is used to define the device pattern. (c) PMMA exposed during the e beam writing process is removed after developing. The sample is then placed in a BOE solution for 15 s to remove SiO_2 layer. (d) A thin layer of gold is sputtered onto the surface. To allow for lift-off, the sputtered layer must be kept to a minimum thickness. (e) A thicker layer of gold is evaporated on top of the sputtered gold layer. (f) Lift-off in hot acetone leaves an intact device with excellent leakage properties.

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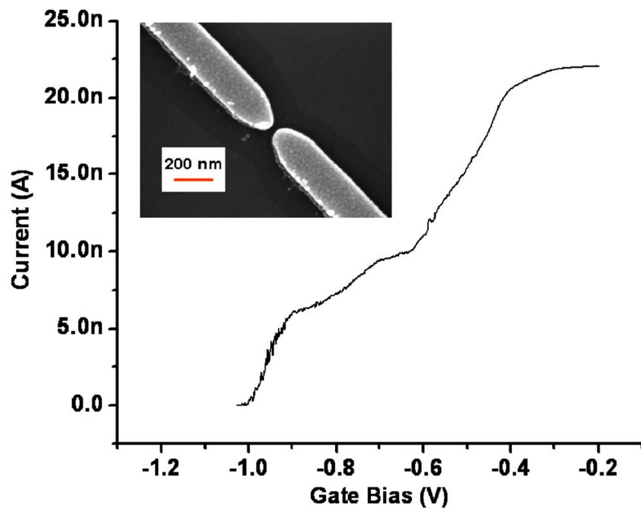

FIG. 3. (Color online) Current through a split gate, fabricated with a sputtered layer of gold, as a function of applied voltage. Stepwise depopulation of edge channels as evidenced through decreasing steps in current, as well as a pinch off voltage around −1.0 V, indicate excellent gate characteristics. Inset: SEM picture of the split gate structure.

We found that if the sputtered layer is thin enough (≲15 nm), it can still be lifted off cleanly. The final devices were produced by using a buffered oxide etch (BOE) to remove the SiO_2 immediately prior to metallization. We then sputter a thin layer (12 nm) of gold onto the surface. After sputtering, a thicker layer of gold (35 nm) is deposited by electron beam evaporation to reinforce the structural integrity of the device. Lift-off was then performed in heated acetone (55 °C) for approximately 2 h (Fig. 2).

Complete pinch off of the current through split gate structures in devices formed by this fabrication technique (Fig. 3 inset) was observed to occur at biases in accordance with Fig. 1(a), indicating a strong coupling between the gate electrodes and the 2DEG. The emergence of more pronounced steps in the depletion curves are due to the depopulation of the one dimensional subband, which is verified by the stepwise edge-channel depopulation in a magnetic field. The stepwise depopulation is evidence of sharp electrostatic confinement beneath the gates. Both the lower operating bias necessary to achieve depletion and the enormous reduction of leakage current lead to a more stable electrostatic environment, which will be necessary for developing the next generation of SiGe based devices.

By using Schottky surface gates formed with sputtered Au, we demonstrated that it is possible to dramatically reduce the leakage current in strained Si/SiGe while simultaneously improving the coupling strength between the gates and 2DEG. The advantages of sputtering, as opposed to thermal or electron beam evaporation, are likely due to the interdiffusion of Au and Si leading to the formation of gold-silicide compounds. A nanofabrication process is developed specifically to enable the fabrication of Au sputtered submicron gates. A split gate device using this technique demonstrates excellent electrostatic characteristics. Advancements in the effectiveness of Schottky gates allow for the continued use of conventional surface gate geometries, superseding the need for more exotic gating techniques.

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