Threshold Error Penalty for Fault-Tolerant Quantum Computation With Nearest Neighbor Communication

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Abstract—The error threshold for fault-tolerant quantum computation with concatenated encoding of qubits is penalized by internal communication overhead. Many quantum computation proposals rely on nearest neighbor communication, which requires excess gate operations. For a qubit stripe with a width of $L + 1$ physical qubits implementing $L$ levels of concatenation, we find that the error threshold of $2.1 \times 10^{-5}$ without any communication burden is reduced to $1.2 \times 10^{-7}$ when gate errors are the dominant source of error. This $\sim 175 \times$ penalty in error threshold translates to an $\sim 13 \times$ penalty in the amplitude and timing of gate operation control pulses.

Index Terms—Fault tolerance, quantum information.

I. INTRODUCTION

A CRITICAL architectural issue for quantum computation is the internal communication of quantum information within the processor. There are a variety of proposed quantum processor implementations with different mechanisms for internal communication. For instance, the linear ion trap proposal of Cirac and Zoller [1] involves physical motion of massive ions for internal communication, as do proposals using more complex ion trap structures [2]. Alternative proposals involve using photons and cavity quantum electrodynamics (QED) for communication [3]. The cavity QED approach has been extended to the solid state [4], [5]. Even direct transport of information carrying electrons has been suggested for the solid state [6], [7].

This paper is motivated by another class of quantum computation proposals that rely upon local communication through nearest neighbor interactions [8]–[10]. For instance, communication among electron spins in semiconductors can be performed with sequential SWAP gate operations, which are generated by a controlled Heisenberg exchange between adjacent electrons. An appealing feature of the SWAP operation is that it is generated by the very same two-qubit interaction used for computational operations. Also, a substantial degree of parallelism can be employed. However, the protection of qubits with concatenated error correction requires communication between a number of physical qubits that grows exponentially with concatenation level. This exponential increase in SWAP operations might suggest that concatenated error correction will fail to reduce the logical qubit error rate. Gottesman [11] and Aharonov and Ben-Or [12] have pointed out that a threshold error exists despite an exponential increase in logical gate count with concatenation level $L$, although no attempt was made to quantify what that threshold might be. In this paper, we estimate that threshold.

The main result we report here is that the number of nearest neighbor communication operations is merely a constant factor over and above the necessary logical operations for error correction at each concatenation level $L$. Our estimated error thresholds are summarized in Table I. We analyzed in detail fault-tolerant error correction with a concatenated 7-qubit Calderbank–Shor–Steane (CSS) code [13], [14] on a linear qubit stripe with a width of $L + 1$ physical qubits for $L$ levels of concatenation and find an $\sim 175 \times$ reduction in threshold gate operation error due to nearest neighbor communication overhead. This translates to a $\sim 13 \times$ increase in accuracy of control pulse amplitude and timing in gate operations. Although nearest neighbor communication incurs a significant penalty in the requisite experimental accuracy of qubit gate operations, it is not a fundamental obstacle to fault-tolerant computation in the solid state. Our analysis is in general agreement with the recent work of Svore et al. [15], who also show that internal communication with local interactions incurs an error threshold penalty, although they do not fully account for all communication steps.

This paper is organized as follows. In Section II, we describe the underlying architecture of a quantum processor composed of electron spin qubits, including a description of the physical layout of electron spin qubits and their grouping into concatenated CSS logical qubits. We describe a fault-tolerant error correction protocol in Section III. Our protocol implements error recovery without direct measurement. In Section IV, we calculate the threshold error for gate operations under our error correction protocol, with various assumptions about available resources. Section V considers the relation between control pulse accuracy and gate error thresholds.

II. LAYOUT ARCHITECTURE

Given the problem of internal communication in a quantum processor, a higher dimensional architecture is preferred because it would allow qubits to be as close as possible. However, there must be access by control wires, thus limiting the packing
TABLE I
GATE COUNT FOR ERROR CORRECTION $N_G + N_{G_c}$ AND FOR LOGICAL CNOT OPERATIONS $N_U + N_{U_c}$ UNDER DIFFERENT ASSUMPTIONS OF INTERNAL COMMUNICATION RESOURCES AND QUANTUM ERROR CORRECTION. APPROXIMATE THRESHOLD GATE ERROR PROBABILITIES ARE GIVEN, AS WELL AS CONTROL PULSE ACCURACY THRESHOLDS (SEE TEXT FOR DETAILS)

| No Communication Overhead | $|0\rangle_L$ Preparation | $|0\rangle_L$ Preparation | $|0\rangle_L$ Preparation | $|0\rangle_L$ Preparation |
|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| No                        | 70                        | 7                         | $3.4 \times 10^{-4}$      | 2.1°                      |
| $|0\rangle_L$ Preparation  | 298                       | 7                         | $2.1 \times 10^{-5}$      | 0.52°                     |
| Remote CNOT Communication | 238                       | 35                        | $2.7 \times 10^{-5}$      | 0.60°                     |
| $|0\rangle_L$ Preparation  | 1090                      | 35                        | $1.6 \times 10^{-6}$      | 0.14°                     |
| SWAP Communication        | 1008                      | 203                       | $1.4 \times 10^{-6}$      | 0.13°                     |
| $|0\rangle_L$ Preparation  | 3754                      | 343                       | $1.2 \times 10^{-7}$      | 0.034°                    |

Fig. 1. Schematic representation showing how the number of available metal wire layers limits the width of a 2-D qubit array to only about 10–20 qubits.

Fig. 2. Requirement for gate electrode access to qubits restricts the layout to stripes of either serpentine or intersecting geometry.

Universal sets of fault-tolerant operations are known only for CSS error-correcting codes of various size [12], [17]–[19]. In our work, we shall consider the CSS code [7], [1], [3]. Concatenation [20], where each logical qubit is composed of encoded qubits, which are in turn composed of encoded qubits and so on, can suppress logical error rate to an arbitrary degree, provided that the physical error rates remain below a threshold value. The self-similarity of concatenation naturally leads to the self-similar logical structure illustrated in Fig. 3. There are seven level $L = 1$ logical qubits forming the CSS codeword that represents a single level $L$ logical qubit $|\psi_L\rangle$. A minimum of two logical zeros, $|0\rangle_L$, and six initially arbitrary ancillae, $|a\rangle_{L-1}$, are required to perform error correction on $|\psi_L\rangle$. We consider $L+1$ parallel lines of physical qubits to implement error correction and computation with $L$ levels of concatenation. The error correction protocol is described in detail in the next section. An important feature of the self-similar hierarchy is that, at each concatenation level, the same qubit protection block is employed.
The key point about the bit-flip indicator block $I$ is that it operates on logical zeros that have effectively measured the logical qubit error, but not the logical qubit itself, by virtue of a logical CNOT gate. As was pointed out by Boykin et al. [22], the identification of which operations require full quantum coherence and which operations do not is important since “quantum” operations require full protection against both phase-flip and bit-flip errors, while “classical” operations require protection against bit-flip errors only. Note from Fig. 5 that the outputs of indicator block $I$ are used only as control bits for the error recovery operations acting upon the logical qubit. Arbitrary phase flips in the output of $I$ have no effect on the logical qubit. Likewise, phase flips on the input of $I$ have no effect on the logical qubit since the syndrome is encoded as bit flips on the input to $I$. We need only to protect against bit-flip errors in $I$, so that the operations within $I$ can be thought of as essentially “classical” in nature, even though they are executed by physical qubit gates. Thus, $I$ can, in principle, be protected with classical fault tolerance, which has been shown to be much more efficient than quantum fault tolerance [23] to ensure that the operations within $I$ will contribute negligibly to the quantum error threshold.

Of course, the requisite logical zeros $|0\rangle_L$ that allow for efficient fault-tolerant error correction are complex entangled states which must be created with low error probability to begin with. One approach to this problem is to dedicate adjacent quantum circuitry whose sole function is to prepare and purify logical zeros, providing a steady supply at various concatenation levels specifically for this purpose. Alternatively, the preparation of logical zeros can be performed directly within the qubit error protection block. The full error-correction circuit is illustrated in Fig. 6. Purification of three $|0\rangle_L$’s, prepared by the $\Omega_L$ block, results in a single $|0\rangle_L$ state for use in error correction. The $\Omega_L$ zero preparation block is given in Fig. 7. Bit-flip errors are corrected with a modified indicator block $I_P$, which also corrects

...
for a possible parity flip error corresponding to the logical zero being in the state $|1\rangle_L$ (and thus requiring a minimum of four ancillae). The qubit protection block must increase in size to accommodate $|0\rangle_L$ preparation in this case. A total of 46 qubits would be required that are arranged in the following sequence of $L - 1$ qubits (compare with Fig. 6): seven qubits for storing $|0\rangle_L$, seven qubits for storing a $|0\rangle_L$, three ancillae $|0\rangle_{L-1}$ for $I_F$, seven qubits for storing a $|0\rangle_L$, four ancillae $|0\rangle_{L-1}$ for $I_F$, seven qubits for storing a $|0\rangle_L$, seven qubits for storing a $|0\rangle_L$, and four ancillae $|0\rangle_{L-1}$ for $I_F$.

IV. ERROR THRESHOLD PENALTY

The number of physical qubits for our concatenated CSS encoding required to store and protect one logical qubit is $27^L$ (or $46^L$, including logical zero preparation). Several levels of concatenation already lead to a large number of physical qubits (although the width of the qubit stripe grows only as $L + 1$). Likewise, the number of physical gate operations grows exponentially ($N^L$), where $N$ is approximately the number of logical operations required at level $L - 1$ in order to implement a single logical function at level $L$. For example, with a single level of encoding, $N$ is simply the number of physical gate operations required to perform some function on our seven-qubit CSS code word (or multiple code words in the case of a multiquubit logical function).

The number of gate operations $N$ will depend on the function being performed. We consider implementing a simple two-qubit unitary $U_L$ followed by error correction $E_L$, as illustrated in Fig. 4(b). Error correction might require $N = N_E$ logical gate operations at level $L - 1$. There will be additional logical SWAP operations at level $L - 1$ that are required to move qubits around, since only nearest neighbor interactions are permitted. We let $N_{Ec}$ be the number of required nearest neighbor SWAP communication operations, which brings the total number of level $L - 1$ operations to $N = N_E + N_{Ec}$. Of course, the unitary $U_L$ will require $N_U$ operations at level $L - 1$, as well as $N_{Uc}$ additional communication operations at level $L - 1$. The total gate operation count at level $L - 1$ to implement $U_L$ followed by $E_L$ is simply $N = N_U + N_{Ec} + N_E + N_{Ec}$. The total physical gate count is again approximately $N^L = (N_U + N_{Ec} + N_E + N_{Ec})^L$, because each of the $N$ operations at $L - 1$ is simply a unitary $U_{L-1}$ followed by error correction $E_{L-1}$. The self-similar hierarchy requires that $N$ operations at $L - 2$ are required for each operation at $L - 1$ and so forth, including communication.

In reality, the gate count $N_U + N_{Ec}$ varies among the various logical qubit operations possible. For instance, Hadamard at level $L$ requires $N_U = 7$ Hadamard gates at level $L - 1$ and $N_{Ec} = 0$ communication gates. In contrast, the gate operations $N_U + N_{Ec} = 7 + 42$ involved in a logical SWAP on the same qubit line are illustrated in Fig. 8 for adjacent logical qubits. Clearly, the value of $N_E$ can be very large, although a substantial fraction of operations at each logical level can be performed in parallel. Note the fault tolerance of the logical SWAP gate: a single swap gate failure induces one error in each logical qubit, which can be recovered independently by error correction. Of course, the extra qubits involved in a qubit protection block increases the number of communication swaps $N_{Ec}$. As a final example, we show the partial sequence of gate operations required for the logical CNOT gate in Fig. 9. It is in implementing the CNOT gate that an additional line of qubits is used for every concatenation level, resulting in a total of $L + 1$ lines of qubits. Similar sequences are used for the SWAP and CNOT gates required for the error-correction operation $E_L$, contributing to $N_E + N_{Ec}$.

Despite the exponential increase in physical qubits and physical gate operations with concatenation level (while the width of the stripe merely grows linearly in concatenation level), logical errors are suppressed double-exponentially with concatenation level. We let $P_j$ be the logical error probability on a first-level encoded state $|\psi\rangle_1$ after a two-qubit unitary followed by a single
and is the probability of physical gate error, which is assumed to be equal for all gates, and of the seven constituent gates, are shown interacting). The logical qubits are suppressed amongst the logical gate operations with remaining. This leads to the error-correction cycle. Likewise, at higher levels now includes the nearest neighbor communication steps. I it, the probability of a logical error is bounded above by 1/3000. While logical error rates shall vary slightly due to differences in code words and error-correction cycle. By the fault-tolerant construction of and, the probability of a logical error is bounded above by 1/100 to 1/105. Thus, for concatenated error correction, we have

\[
P_L \leq \left( \frac{N}{2} \right) P_{L-1}^2 \approx \frac{N^2}{2} P_{L-1}^2 \]

(2)

which leads to \(P_{L-1} < 2/N^2 = P_{th}\), being the error threshold condition for all \(L\). The corresponding required phase accuracy for gate operations, as described in Section V, is \(\phi = 2\sqrt{2}/N\). From the above relations, we arrive at the standard logical error probability for concatenated error correction

\[
P_L \leq P_{th} \left( \frac{\epsilon}{P_{th}} \right)^{2^L} \]

(3)

but where \(N\) now includes the nearest neighbor communication overhead at a particular concatenation level. The exponent \(2^L\) results in an overwhelming super-exponential in \(L\) suppression of logical errors, while the number of qubits and gate operations increases only exponentially in \(L\).

Suppose that a quantum computation requires a sequence of \(T\) logical gate operations, then a logical error probability \(P_L = 1/T\) will give the correct result with only several trials of the computation. The relation between the maximum number \(T\) of operations in a calculation and concatenation level \(L\) can be written

\[
T = \frac{1}{P_L} \geq \frac{1}{P_{th}} \left( \frac{P_{th}}{\epsilon} \right)^{2^L} \]

(4)

or alternatively

\[
L \leq \log_2 \left( \frac{\log_2(TP_{th})}{\log_2(P_{th}/\epsilon)} \right) \]

(5)

For instance, the error threshold might be \(P_{th} = 10^{-6}\), while the physical gate operation error is an order of magnitude better at \(\epsilon = P_{th}/10 = 10^{-7}\). We then have an accessible computation length \(T = 10^6 \times 10^{22}\), which, for \(L = 3\), gives \(T \geq 10^{14}\). It follows that interesting calculations can be performed with only a few layers of concatenation (i.e., a qubit stripe with a width of only a few qubits) if physical error probabilities well below the error threshold can be achieved.

The problem of estimating error threshold has been reduced to counting gate operations, for which our numerical results are summarized in Table I. Note that we have neglected storage errors in our present analysis since the coherence times of electron spins in semiconductors [24] exceed the expected gate operation times by at least ~8 orders of magnitude, with further improvement expected. The top row of Table I gives the most favorable error thresholds where any qubit can interact with any other qubit without any extra communication operations. The bottom row is the least favorable case where nearest neighbor SWAP operations are used on a linear qubit array to implement all operations. The middle row represents an intermediate case, where the remote CNOT is used to perform a CNOT gate between distant qubits [25], [26]. The remote CNOT requires a shared Einstein–Podolsky–Rosen (EPR) pair, which is a resource that might be generated by independent hardware with sufficient purity that the EPR error rate contributes negligibly to the overall error rate of the remote CNOT and the error threshold. Measurement and classical communication are also required for the remote CNOT (see the Appendix).

For all three communication schemes, the gate count is given in Table I for subcases where \(|0\rangle_L\)’s are supplied by adjacent circuitry (e.g., a parallel qubit stripe) or where the \(|0\rangle_L\)’s are prepared directly within the error-correction circuit itself (as in Fig. 6), thus burdening the error threshold. In the former case, we assume that the adjacent circuitry can prepare and purify logical zeros to reach an error probability much less than the preparation circuit of the former case, thereby contributing to the error threshold negligibly. This might be achieved by successive rounds of purification.

In all cases, we assume that those portions of the circuit that can be implemented with classical fault-tolerant logic [22], albeit with qubit gates, take advantage of the greater efficiency of classical coding. The threshold error for classical fault-tolerant circuits has been estimated to be between ~1/100 to ~1/3000 depending on topology and communication resources [23]; therefore, we assume that the error rates in the classical circuits are negligible compared to the quantum circuits, so that in counting the gate operations we can neglect the operations in \(I\)
and $I_T$. Furthermore, the dual-control phase flip ($\Lambda_2(Z)$) and dual-control bit flip ($\Lambda_2(X) = Toffoli$) are assumed to count merely as two-qubit interactions, since fault-tolerant classical logic can be used to generate a single classical control bit. The remaining sundry details involved in counting gate operations are left to the Appendix.

Observing the gate error thresholds in Table I, we see that SWAP communication incurs a penalty of $\sim175 \times$ compared to the case of free communication. Communication through the remote CNOT incurs a penalty of $\sim12 \times$ compared to the free communication case. The improvement associated with remote-CNOT communication is not as much as one might expect, since the remote CNOT requires multiple operations proportional to the size of the logical qubits. Thus, internal quantum communication reduces gate error thresholds for fault-tolerant computation by a substantial factor that we estimate to be from $\sim12 \times$ to $\sim175 \times$. While this certainly increases the difficulty in experimentally realizing fault-tolerant gate operations, it is by no means an impasse for solid-state quantum computation, as we discuss in Section V.

V. ERROR PROBABILITY AND GATE OPERATION ACCURACY

So far, we have worked entirely with error probabilities. In practice, experimental gate accuracy is more naturally specified in terms of control pulse amplitude. Consider the spin (or a qubit pseudospin), illustrated in Fig. 10. Suppose a control pulse, as is used in spin resonance, was to bring the spin into alignment with the $x$ axis. However, an error in pulse area, phase, or timing may cause a misalignment by some small angle $\phi$. The probability of error $\epsilon$ is then the probability that the spin is not projected into the $+x$ direction when a measurement is performed along the $x$ axis. The probability of projection along the $+x$ direction is $\cos^2(\phi/2)$, so that the error probability is

$$\epsilon = \sin^2(\phi/2) \approx (\phi/2)^2. \quad (6)$$

The required gate timing and amplitude accuracy is $\phi = 2\sqrt{\epsilon}$, which is specified as a phase angle, is proportional to the square root of the threshold error probability. The gate accuracy thresholds are given in degrees in Table I. Of course, the $\sim12 \times$ to $\sim175 \times$ penalty in error probability threshold becomes only a $\sim3.5 \times$ to $\sim13 \times$ penalty in control pulse accuracy. In order to achieve an error probability of $10^{-7}$, one would require about 1/30 of a degree accuracy in control pulse timing, which is not entirely infeasible since it would require about 1-ps phase accuracy in a clock period of about 10 ns. Recall that an error probability of $10^{-7}$ for a quantum processor with threshold error probability $10^{-6}$ and three levels of concatenation will allow a computation with $\geq 10^{14}$ operations. Thus, thinking about gate errors in terms of phase angle makes it clear that very small error probabilities are achievable.

VI. CONCLUSION

Internal quantum communication remains a challenging architectural problem that impacts the threshold error for fault-tolerant computation with encoded logical qubits. The communication operation overhead required to distribute information among a number of qubits that grows exponentially with concatenation level can be a significant burden. Whether one is limited to nearest neighbor communication, a communication bus (as in the original Cirac–Zoller ion trap proposal [1]), or communication by modified teleportation schemes such as the remote CNOT, there is always a communication penalty in error threshold. The minimum communication overhead cost is associated with a communication bus, where a single operation for “transmitting” and a single operation for “receiving” is possible in principle. The question of whether a sufficiently robust communication bus is available for solid-state qubits remains open. Ballistic transport of electron spins through mesoscopic wires is predicted to give error rates of $\sim0.6$ for GaAs [7], far above our stated threshold requirements even for the free communication case. Much more promising is the combination of cavity QED techniques with confined electron spins [4] or superconducting circuits [5], where an electromagnetic bus can couple a number of qubits. The error rates of such a bus, the reconfigurability of its links, and its parallelism (i.e., how many qubits can be transported simultaneously or through the same link) must all be carefully considered in determining what benefits, if any, we can expect over nearest neighbor architectures. Nonetheless, we expect that communication overhead can be mitigated to a large extent by circuit optimization. Recent work [27] on laying out Shor’s factorization algorithm on a linear chain of qubits under the restriction of nearest neighbor interaction has shown that circuit optimization can greatly reduce the number of logical qubit SWAPs required.

APPENDIX I

THRESHOLD ERROR CALCULATIONS

We provide a brief summary here of the counting of gate operations, which then leads to the threshold error. Error correction at concatenation level $L$ with the circuit $E_L$ requires the use of both single-qubit unitaries and two-qubit unitaries at levels $L$ down to the physical layer. Interestingly, the quantum portions of the circuit $E_L$ (see Figs. 5 or 6) consists of gate operations that are directly fault-tolerant, where qubit-wise (or transversal) operations are sufficient. These operations include CNOT, SWAP, and Hadamard rotation (H). The control bits of the dual control gates are classical, so a full quantum Toffoli is not required. Of course, indirectly fault-tolerant gates such as...
the Toffoli ($\Lambda_2(X)$) or $\pi/8$ rotation ($Z^{1/4}$) are required for universal computation. We do not calculate the error threshold for indirectly fault-tolerant gates here.

A. Free Communication

First, we consider the idealized case where communication is achieved without any extra operations, in other words, any two qubits can interact directly at any time. In this case, $N_{U,C} = N_{E,C} = 0$, and we need only count the number of computationally useful gates. A directly fault-tolerant two-qubit unitary will require $N_E = 7$ operations. The error correction gate count without logical zero preparation is

$$N_E = 4 \times 7\text{CNOT} + 4 \times 7H + 7\Lambda_2(X) + 7\Lambda_2(Z) = 70 \tag{7}$$

where the $L - 1$ gate type and count are indicated. With logical zero preparation, we have

$$N_E = 70 + 12 \times 0_L + 4 \times 7\Lambda_2(X) + 8 \times 7\text{CNOT}$$

$$= 298 \tag{8}$$

where again $L - 1$ gate type and count was indicated.

B. Remote-CNOT Communication

Next, we consider the intermediate communication case involving remote-CNOT operation, which we abbreviate as reCNOT. The reCNOT circuit is indicated in Fig. 11. For simplicity, we assume that the classical communication and EPR preparation introduce negligible errors compared to the other gate operations involved. We see that a reCNOT between two level $L - 1$ qubits requires five level $L - 1$ operations, so that a reCNOT between two level $L$ qubits requires $N_{U,C} = 5 \times 7$ level $L - 1$ operations. The error correction gate count without logical zero preparation becomes

$$N_E = 4 \times 7\text{reCNOT} + 4 \times 7H + 7\Lambda_2(X) + 7\Lambda_2(Z)$$

$$= 140 + 28 + 35 + 35$$

$$= 238 \tag{9}$$

where $\Lambda_2(X)$ and $\Lambda_2(Z)$ are counted as reCNOT operations (recall that they can be implemented with single classical control bits). With logical zero preparation, we have

$$N_E = 238 + 12 \times 0_L + 4 \times 7\Lambda_2(X) + 8 \times 7\text{reCNOT}$$

$$+ 140 + 280$$

$$= 1090 \tag{10}$$

where we have made use of both nearest neighbor CNOT and reCNOT in the logical zero preparation.

C. SWAP Communication

Finally, we consider communication by SWAP gates. Without logical zero preparation, a level $L$ qubit protection block is $27$ $L - 1$ qubits long. Applying CNOT between two level $L$ qubits as in Fig. 9 requires $N_U + N_{U,C} = 203$ level $L - 1$ operations on each logical qubit argument. The error-correction operation requires

$$N_E = 4 \times (7\text{CNOT} + 112\text{SWAP})$$

$$+ 4 \times 7H + 2 \times (7\text{SWAP} + 84\text{SWAP})$$

$$+ (7\Lambda_2(X) + 154\text{SWAP}) + (7\Lambda_2(Z) + 154\text{SWAP})$$

$$= 1008 \tag{11}$$

where we note that 112 communication SWAPs are required for applying CNOT between $|0\rangle_L$ with an adjacent $|0\rangle_L$, and 84 communication SWAPs are required for logical swapping of a $|0\rangle_L$ with another $|0\rangle_L$ taking account of the extra ancilla $|0\rangle_{L-1}$ in the way.

When logical zero generation is included, the qubit protection block increases in size to 46 qubits. Applying CNOT between two level $L$ qubits now requires $N_U + N_{U,C} = 343$ level $L - 1$ operations because of the increased size of the qubit protection block. The error correction operation requires

$$N_E = 1008 + 12 \times 0_L + 2 \times (7\text{SWAP} + 84\text{SWAP})$$

$$+ 4 \times (7\text{SWAP} + 98\text{SWAP}) + 4 \times (7\text{CNOT}$$

$$+ 112\text{SWAP}) + 4 \times (7\text{CNOT} + 168\text{SWAP})$$

$$+ 4 \times (7\Lambda_2(X) + 154\text{SWAP})$$

$$= 3754 \tag{12}$$

where we note that each logical $|0\rangle_L$ generation requires 27 level $L - 1$ operations (Fig. 7), and the SWAP communication accounts for all extra ancilla $|0\rangle_{L-1}$ in the way.

ACKNOWLEDGMENT

The authors would like to thank I. Chuang for bringing the issue of internal communication in quantum computation to our attention. The authors also thank D. Gottesman for pointing out an error in an earlier manuscript.

REFERENCES

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