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NOTE

FLEXIBLE, THIN-FILM, GaAs HETERO-JUNCTION BIPOLAR TRANSISTORS MOUNTED ON NATURAL DIAMOND SUBSTRATES

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1. INTRODUCTION

Thermal considerations become important for optimal operation of high power heterojunction bipolar transistors (HBTs) in applications such as the next generation of phased-array radar systems. In particular, devices grown on GaAs substrates suffer due to the mediocre thermal conductivity of the III–V compound semiconductors. The maximum achievable power density before device performance degrades is mainly limited by the junction temperature. As a consequence, a great deal of interest has arisen[1,2,3] in determining both the experimental and theoretical temperature profile in GaAs ICs. Nevertheless, these thermal constraints can be greatly alleviated using alternative packaging concepts for removing the excess heat[4].

With the recent advances in thin film handling and manipulation technologies, the active layers of electronic circuitry can be separated from their substrates on which they were synthesized and furthermore mounted onto different types of substrates with suitable thermal properties. Yablonovitch *et al.*[5] have demonstrated the bonding of GaAs epitaxial films onto arbitrary substrates using epitaxial lift-off (ELO) and palladium bonding techniques. This process relies on the extremely high etching selectivity between the substrate and a sacrificial or release layer[6]. Another similar process consists of back etching the substrate up to an etch stop layer and is hereafter referred to as the total substrate removal (TSR) technique. The resulting thin film can be transferred and bonded onto an efficient heat sinking substrate.

Natural type IIA diamond has a thermal conductivity, $K_{\text{th-diamond}}$ of 20 W/cm/K, or 40 times greater than the thermal conductivity $K_{\text{th-GaAs}}$ of GaAs. Recently, using TSR techniques with a combination of mechanical and CF_4 plasma etching, Sullivan *et al.*[7] have transferred AlGaAs/GaAs heterojunction bipolar transistors (HBTs) onto CVD grown diamond and observed a significant drop in the total thermal resistance. In their work, a 500 nm thick layer of indium solder served as a bonding inter-layer between GaAs and the polycrystalline CVD diamond substrate. To investigate the ultimate thermal performance which may be achieveable, in the present work we transfer AlGaAs/GaAs HBTs directly onto natural, single crystal, type IIA diamond substrates, limited only by a 10 nm Pd inter-layer.

2. BONDING AND TRANSFER PROCESS

The transistors are fabricated as test transistors in conjunction with, and interspersed among, high speed III–V heterojunction bipolar integrated circuits. The detailed structure of these AlGaAs/GaAs HBTs can be found[8] elsewhere. Prior to integrated circuit processing, and before the growth of the collector layer, a thin epitaxial $Al_{0.8}Ga_{0.2}As$ release layer is deposited. The distance between the base–collector junction and this release layer is approx. 1.3 μm. Due to the specific layout of the multiple metallization layers in these integrated circuits, the metal interconnect lines were not protected from the acid as would have been needed for use of the epitaxial liftoff technique. Therefore it was necessary to use the total substrate removal (TSR) process instead, employing the $Al_{0.8}Ga_{0.2}As$ layer as an etch stop layer, rather than as a release layer. Although the circuit masks were not originally designed for ELO processing, minor changes in the integrated circuit layout could have permitted us to perform epitaxial liftoff.

The TSR process consists of the following procedure: Apiezon wax is deposited on the circuit face of a GaAs wafer, protecting the active devices. The substrate is then etched away in an H_2O_2/NH_4OH bath. The etch rate as well as the selectivity between the GaAs substrate and the $Al_{0.8}Ga_{0.2}As$ etch stop layer are dictated by the NH_4OH concentration. In a 1:10 H_2O_2:NH_4OH solution, the GaAs etch rate is around 5–6 μm/min at room temperature and the selectivity is above 200, corresponding to an etch rate of <0.025 μm/min for the $Al_{0.8}Ga_{0.2}As$ etch stop layer. The etching mechanism involves the growth of a surface oxide layer that is subsequently etched away. Consequently, to assist the removal of the oxide layer, the solution is stirred vigorously. After the GaAs is fully stripped away, the $Al_{0.8}Ga_{0.2}As$ etch stop layer is removed in a dilute HF solution.

At this stage of the processing we rinsed away the wax in trichloroethylene and found, to our surprise and delight, that the polyimide insulation layers, which are formed as part of the conventional IC processing, are strong enough to mechanically support the *free standing* integrated circuits. Like most polymers, these organic layers contract relative to the monomer upon polymerization, and remain under tensile stress on the integrated circuit. When the integrated circuits are detached from their substrates, the strain is partially relieved and the thin film integrated circuits become slightly curled. In addition there are slight undulations in the *free-standing* GaAs films associated with specific circuit patterns. This flexible sheet, only microns thick, is easily handled with regular tweezers and requires no particular precautions. Indeed, the measured current–voltage (I–V) characteristics of the *free-standing* HBTs suggest that no additional crystalline defects such as dislocations were introduced during the handling procedure.

In the final packaging configuration the circuits are mounted on type IIA natural diamonds which are $3 \times 3 \times 0.25$ mm in size, cut and polished on the [110] face. Since GaAs does not adhere well to diamond, the as-polished diamond surface is first coated with an extremely thin (5 nm) layer of Cr followed by only 10 nm of evaporated Pd. Thicker metallization layers would add additional thermal resistance and considerably reduce the heat sink efficiency. The GaAs–Pd bond has the advantage of being an excellent thermal contact in addition to being mechanically robust[9]. The HBTs are then transferred onto the diamond in a deionized water environment and placed under mechanical

pressure for 24 h in order to help squeeze out the excess water [5] and to flatten the non-planar semiconductor film. In order to strengthen the metallurgical bond, the samples are further annealed at 200°C for 30 min in a N_2 ambient. A "Scotch adhesive tape pull test" tears the metallization layers off the integrated circuit, but the semiconductor film remains bonded to the diamond except in the microscopic vicinity of trapped dust particles.

3. RESULTS AND DISCUSSION

Small, medium and large emitter size test transistors were studied, with areas of 4.2 μm^2 (1.4 × 3 μm), 175.95 μm^2 (two rectangles of 6 × 23 μm and 2.3 × 16.5 μm arranged in a Tee configuration), and 4489 μm^2 (67 × 67 μm), respectively. The measured static I–V characteristics of a large and medium size HBT are shown in Fig. 1(a) and (b), respectively. The measurements were performed with the samples resting on a copper block at ambient temperature. The base current was increased in steps of 64 μA, from 0 to 256 μA. For comparison purposes, the same transistor was measured before and after bonding. The roll-off and negative differential resistance (NDR) in the collector characteristics at high power are known to be associated with the substantial increase in the junction temperature[10]. This effect is accompanied by a reduction of the d.c. current gain, β, as the collector–emitter voltage, V_{CE}, increases. For transistors on diamond, solid lines in Fig. 1, the I–V curves become horizontal and NDR is no longer observed. On the other hand free-standing transistors, the dotted lines in Fig. 1, show extremely poor I–V curves. In the free-standing transistor case, the backside of the HBT rests loosely on a microscope glass slide with very poor thermal conductivity ($K_{th} \approx 0.016$ W/cm/K). The fact that the trend in NDR is reversible, is a convincing proof of the high efficiency of the diamond substrate in cooling the junction temperature. Surprisingly, these changes in I–V curves are more pronounced for the large area transistors. Although at first glance the trend looks puzzling, a more detailed analysis explains the experimental results.

The total resistance to the heat flow can be represented as a number of thermal resistances in series corresponding to the GaAs layer, the diamond heat sink and the microscope slide, respectively. It is worth noticing that since the emitter areas are very small compared to the GaAs or/and the diamond substrates, the latter can be regarded as semi-infinite heat-sinks. A simple model analogous to Ohm's Law[11] can help us in evaluating the total thermal resistance of the system. The heat flux density is given by the well-known Fick's law for heat diffusion:

$$J = \frac{Q}{A} = -K_{th}\frac{\partial T}{\partial r}, \tag{1}$$

where J is the heat flux density, Q the heat flux, A the emitter area, T the temperature, and r the distance from the heat source or the emitter–base junction in the present case. The thermal resistance is defined as the ratio between the heat flux and the temperature and is expressed by:

$$R_{th} = \frac{\Delta T}{Q}. \tag{2}$$

For the very small transistors, the semiconductor junction can be regarded as a point source of heat and eqn (1) is readily solved using hemispherical coordinates. For the large transistor, the total resistance can be divided into the sum of a linear, a cylindrical, and a hemispherical resistance. For simplicity, the dependence of the thermal conductivity, K_{th}, on temperature is neglected. For the large size HBT, the thermal resistance of the device mounted on diamond is calculated to be reduced by a factor of 15 compared to the thermal resistance of the same device on a GaAs substrate. However, the reduction in thermal conductivity for the medium and small emitter size transistors is only by a factor of 6 and 1.5, respectively. These modeling results are in close agreement with the experimental data in Fig. 1(b) where the gain compression in the medium size transistor is only moderately affected. A finite difference three dimensional model[1] indicates that most of the temperature drop occurs in the vicinity of the heat source. In other words, the flow of heat encounters most of its resistance in the 1.3 μm thick sub-collector GaAs layer for small devices and the diamond heat sink plays only a minor role in the heat dissipation process, thus explaining the slight improvement for small HBTs.

In order to better appreciate thermal effects on the electrical properties of the HBTs it is necessary to evaluate the temperature dependence of β. The current gain, β, of n–p–n HBTs as primarily limited by emitter injection

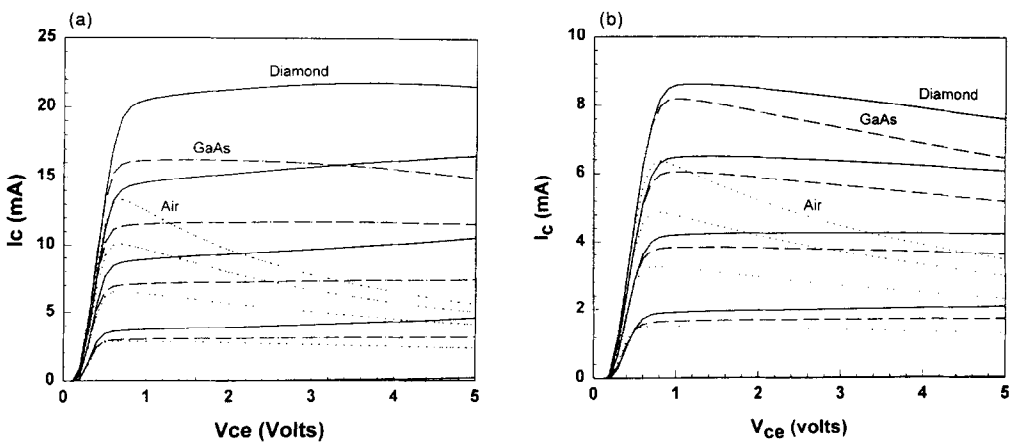

Fig. 1. Static current–voltage characteristics of the large (a) and the medium (b) emitter size HBTs. The emitter areas are 4489 and 175 μm^2, respectively. Base current is increased in steps of 64 μA, from 0 to 256 μA. The straight, dashed, and dotted lines correspond to the HBTs on the diamond substrate, on the original GaAs substrate, and the free-standing HBTs, respectively. For the medium size transistor (b), the thermal performance is only slightly improved by the diamond substrate. The high thermal resistance of the 1.3 μm GaAs sub-collector accounts for most of the temperature drop.

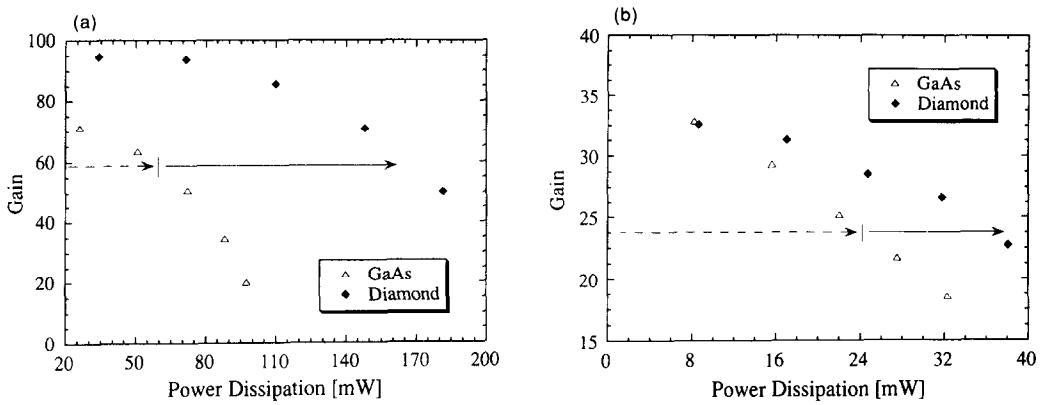

Fig. 2. d.c. current gain, β, vs the power dissipation for the large (a) and the medium (b) emitter size HBTs. The base current is set at 256 μm for both. A factor 3 improvement in the power is obtained for the large size transistor bonded onto a natural diamond substrate.

efficiency is expressed as the ratio of the electron current, J_n, to the hole current, J_p, and is given by:

$$\beta = \frac{J_n}{J_p} = \frac{N_e}{P_b}\frac{v_{nb}}{v_{pe}}\exp((qV_p - qV_n)/kT), \quad (3)$$

where N_e and P_b are the emitter and base doping concentrations, v_{nb} and v_{pe} are the effective velocities of the electrons in the base and the holes in the emitter, and qV_p and qV_n the heights of the potential energy barrier for holes and electrons[12]. With the elimination of the conduction band spike by compositionally grading the emitter, as it is the case for the present HBTs under investigation, the potential energy barrier and hence the thermal activation energy for the holes is greater than that for the electrons. As a natural consequence, the current gain will decrease as the junction temperature increases.

The d.c. current gain, β, is plotted vs the power dissipation in Fig. 2(a) and (b) for the large and medium size transistors, respectively. The base current was kept constant at 256 μA for both the large and the medium size HBTs. At a power level of 60 mW, the gain of the large HBT on GaAs drops by approx. 30%. More importantly, notice the substantial enhancement of the operating power by more than a factor of three between the HBT on GaAs and on diamond. At low power density, the large HBT already shows some gain compression due to the significant thermal resistance of the GaAs substrate. On the other hand, such a dramatic change is not observed for the medium size HBT. Thus, we can see AlGaAs HBTs can function as highly sensitive, microscopic, "thermometers".

4. CONCLUSIONS

A new technique based on the transfer and the bonding of high power thin film transistors onto diamond substrates has proven to be successful in effectively reducing the thermal resistance of the device. However, the resulting improvement in the current gain was more pronounced for HBTs with large emitter size. Nevertheless, the present technique is naturally extensible to high power GaAs ICs and is very promising towards the development of novel packaging schemes with desirable heat sinking properties.

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