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DIRECT BONDING OF GaAs FILMS ON SILICON CIRCUITS BY EPITAXIAL LIFTOFF

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Abstract—Epitaxial liftoff has emerged as a viable technique to integrate GaAs with silicon. The technique relies on the separation of a thin epi-GaAs film from its substrate followed by direct bonding of the thin film to a silicon substrate. The silicon substrate has to meet certain planarity and smoothness conditions in order to obtain high quality bonding. Unfortunately, processed silicon IC chips do not satisfy these conditions. In this paper, we report on the results of two different planarization techniques, plasma etch back and chemical–mechanical polishing, to integrate GaAs LEDs with silicon circuits using epitaxial liftoff. 4 by 8 arrays of GaAs LEDs have been integrated with silicon driver circuits using plasma etch back. We also have lifted off areas as large as 500 mm^2 and bonded them on 5″ device wafers by chemical–mechanical polishing. This can be essential for mass production of optoelectronic devices based on epitaxial liftoff.

1. INTRODUCTION

Silicon integrated circuit technology has been a major factor for the computer revolution in information processing and control. Another important development is that of III–V photonic devices such as semiconductor lasers. The marriage of these two technologies is a goal whose impact will be far reaching. Such a marriage will allow design of high performance processors that utilize the best attributes of silicon and III–V technologies.

Although the complexity of the circuitry depends very much on the type of application, most of the proposed optical processors require several hundred to several thousand transistors in each processor [1,2]. Silicon is the only technology today that can deliver such a large array of processors in a plane with a finite yield. Unfortunately, efficient light sources cannot now be made from silicon as it is an indirect bandgap material. Thus, a technique needs to be developed to integrate silicon with light-emitting materials such as GaAs. Such a technique has to deliver high-performance components with acceptable yields.

A direct approach to integrate silicon with GaAs is hetero-epitaxy using MOCVD or MBE. There are two problems with this approach. First, a silicon foundry process has to be developed to allow such growth in conjunction with partially processed Si circuits. This will be time consuming and expensive. Secondly, the grown materials suffer from crystal defects, including dislocations resulting in degrading device performance and yield. Therefore, flip-chip bonding has been widely used for the integration of Si and GaAs materials. Although it is not a monolithic approach, it has been the only reliable technique that can deliver devices to build large scale optoelectronic systems.

In this paper, we report an alternative technique, Epitaxial Liftoff (ELO), that can be regarded as a semi-monolithic approach. With this technique, a thin film of GaAs is separated from its substrate and then transferred to the top surface of silicon circuits. This way, it is possible to produce three-dimensional OEICs where the top layer contains light sources. These light sources are vertically interconnected to underlying silicon circuits. The ease of application of ELO to Si/GaAs, lithographic alignment, and semi-monolithic high yields obtained with this technique can make it superior to flip-chip bonding.

2. EPITAXIAL LIFTOFF

The details of the ELO process can be found in Refs [3,4]. It has been widely used by many laboratories to demonstrate novel devices[5–9]. The process is illustrated in Fig. 1. There are two important steps in the process. The first one is the removal of a thin GaAs film from a substrate and the second step is the transfer of this film onto a different substrate. The first step relies on the fact that the etch rate of AlAs is much faster than $Ga_{1-x}Al_xAs$ in HF. Therefore, a sacrificial layer of AlAs is grown between the GaAs heterostructure and its substrate. A thick Apiezon W wax on the top of the heterostructure gives the thin film some mechanical strength and handling

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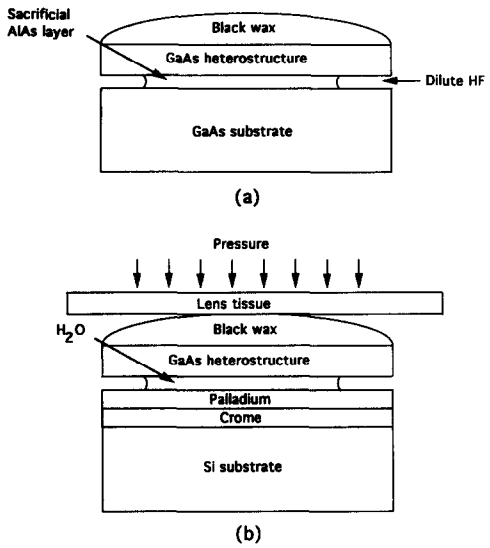


Fig. 1. The illustration of ELO process: (a) separation of thin film from its substrate; (b) bonding of the thin film onto another substrate that is coated with Pd.

capability after detachment from its substrate. Excess wax is removed from sample edges by grinding or by simply cleaning it with trichloroethylene to expose the AlAs sacrificial layer to 10% HF etching solution. Another, more desirable, way to expose the AlAs is to pattern wax with a hot blade followed by wet etching. This technique is described in Section 3.2.1. The sample is then left for several hours in this dilute HF to remove the sacrificial layer. The thin film separates from its substrate upon etching of the AlAs sacrificial layer. Following the further dilution of the HF acid with DI water, the film is picked up with a vaccum tweezer and transferred on to a different substrate such as a processed silicon wafer.

The second step is the bonding of the III–V thin films onto silicon substrates. This is the more critical step as the quality of adhesion affects yield directly. Ideally, a thin film of strong adhesive would be necessary to achieve a good bonding. However, there are several strict requirements on the properties of such an adhesive: It has to be thin enough to avoid step coverage problems when silicon circuits and GaAs devices are connected to each other, it has to withstand later fabrication steps that are needed to make electrical contact to light emitting devices after the film transfer (temperatures up to 400°C), and finally it has to have good thermal conductivity. Instead, we do glueless bonding. The nature of the bonding mechanism depends on the type of substrate surface the film has been transferred to. It has been attributed to Van der Waals forces in the case of SiO_2 and polyimide substrates. Unfortunately, the adhesion can be incomplete due to the weak nature of these forces. This partial adhesion can be a much more severe problem if the film has to be processed

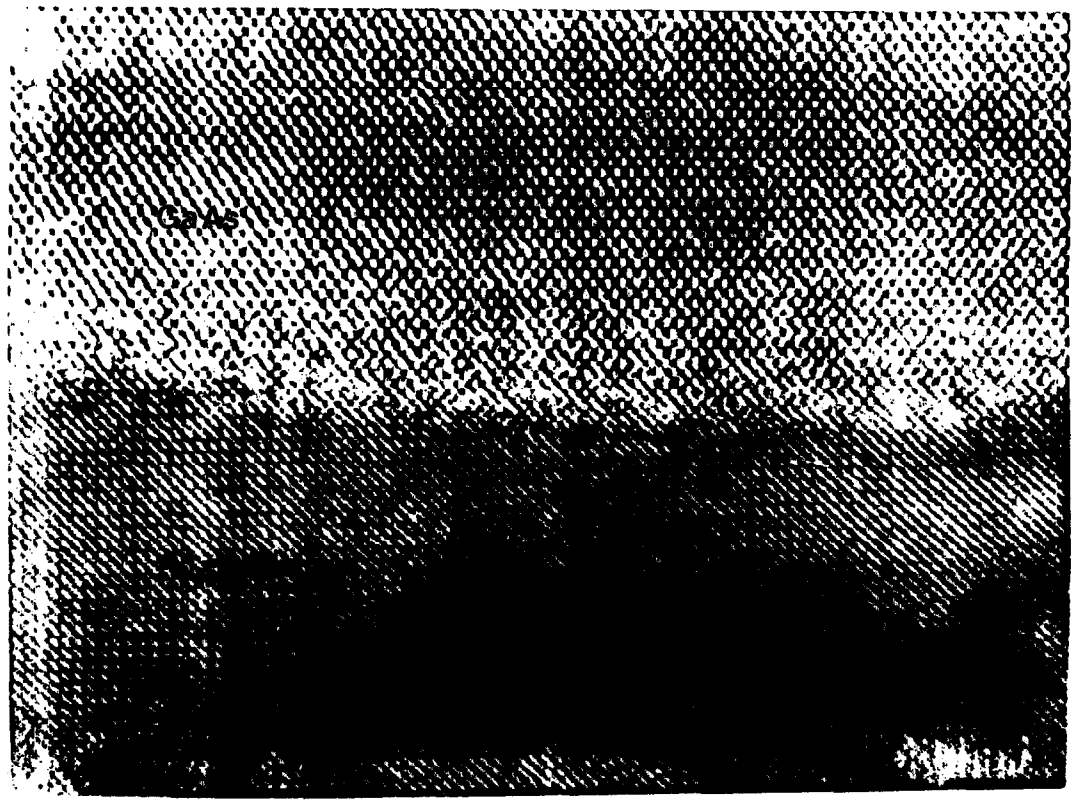


Fig. 2. The TEM cross section of the Pd/GaAs interface. The sharp transition region without intervening oxide layer indicates the high quality of bonding mechanism between GaAs and Pd_4GaAs.

after bonding. During post-fabrication, the film would be more vulnerable to steps such as blow drying, photoresist removal, etc.

A much better bonding can be achieved if the substrate is covered with Pd[10]. GaAs alloys with Pd even at room temperature, forming the intermetallic compound Pd_4GaAs. The result is an excellent bond that survives the "scotch tape test". The bond strengthens rapidly if samples are annealed at 200°C in N_2 ambient for an hour. It has also been found that metallurgical bond becomes stronger if samples are left under ambient conditions for several days. Figure 2 shows the TEM cross section of Pd/GaAs interface. As it can be seen from the smooth transition region (Pd_4GaAs), Pd seems to be the perfect "glue" that is required to achieve successful bonding of thin films on various substrates. Besides being the perfect glue, Pd offers some additional important advantages: It makes a good ohmic contact to p-type GaAs. This makes it possible to use Pd coated substrate as the bottom contact to GaAs devices. Being a metal, Pd can also be used as a heat sink for high power GaAs devices.

The III–V films can be pre-processed or post-processed relative to the bonding step. In the pre-processed case, fully fabricated devices exist in the film before liftoff and the thin film has to be aligned with respect to features on the substrate it will be bonded to. In the post-processed case, the unprocessed film is bonded to a substrate requiring no precise alignment. All the device fabrication is done after bonding. The disadvantage of this technique is that it demands good adhesion during thermal processing. However, this has not been a problem with the strong bond obtained from Pd/GaAs interface. Therefore, the work in this paper is based on post-processing of devices after bonding to a Pd coated substrate. This way, the problem of aligning existing devices with respect to circuit features in the silicon substrate has been eliminated.

The substrate has to meet certain smoothness and planarity conditions to obtain good adhesion of GaAs films. Thin films can stretch over steps that are within the "3 deg condition"[11]. That is, the slope of the surface should not exceed 3 deg from normal at any given point on a substrate. For example, this corresponds to a height difference of 0.05 μm between the points that are separated from each other by 10 μm. This "3 deg condition" makes the requirements on global planarization less strict as long as local planarity is satisfied across a wafer. A typical silicon chip has up to 3 μm steps with a varying spatial frequency. Therefore, it is essential to develop a general planarization technique that is independent of the topography of underlying layers. The substrate smoothness and planarization is so important that the ELO yield is limited to a great extent by the quality of finished surfaces. The next section will review ELO results obtained on surfaces planarized using different techniques.

3. ELO ON PLANARIZED SURFACES

Planarization is an important issue in multilevel metal processes where the insulator thickness between two metal layers has to be controlled with great accuracy to satisfy requirements related to Ultra Large Scaled Integration (ULSI). The limited depth of focus (DOF) of exposure tools for optical lithography has been the major driving force behind planarization requirments. DOF requirements are a function of exposure wavelength and lithographic resolution. For example, DOF is limited to 0.38 μm at 240 nm for a minimum feature size of 0.3 μm[12]. This obviously makes the planarization of interlevel dielectrics a very important part of the entire process. Therefore, a large variety of techniques have been developed. Some of these techniques are becoming a standard step in the fabrication of ICs and are widely used by most of the major foundries. Two different planarization techniques were chosen to demonstrate ELO: The first one is Plasma Etch Back (PEB) and it was used for small size silicon chips (5 by 7 mm for example). The second technique is Chemical Mechanical Polishing (CMP) and it is generally restricted to large wafers (4" and larger). This is due to the fact that all the commercial polishing machines are designed for large size wafers to match standard IC foundry sizes. In this section, PEB and CMP will be briefly reviewed.

3.1. Plasma etch back

In PEB, the sample is first spun with 3–4 μm thick polyimide (PI). It is then coated with a very thick photoresist (PR) layer so that the final surface is almost planar independent of the silicon chip topography (Fig. 3). Although one can initially start with a very thick layer of PI, severe cracks were seen after exposing PI to plasma for a long time. A combination of PI and PR tends to reduce these cracks, if not completely eliminate them. The sample is then put in an O_2 plasma and etched down all the way to the photoresist/polyimide interface. As the etch ratio of photoresist and polyimide can be made very close to each other by adjusting the etching conditions (1:0.95 in our experiments), one would eventually end up with a planar surface if the etching is carried out until the photoresist has been removed entirely. This technique can be applied as many times as necessary until the desired planarity has been reached. Very smooth surfaces (0.01 μm surface roughness over a 3 μm distance) have been achieved using this technique. DEKTAK measurements and visual inspections with a microscope will determine whether the surface is planar enough to allow high quality film bonding. A very good indication of desired planarity can be obtained by visual inspection after Pd evaporation onto planarized surfaces. Basically, at this stage samples should like a flat mirror and one should not be able to see any features of the silicon circuitry under the Pd thin film coating.

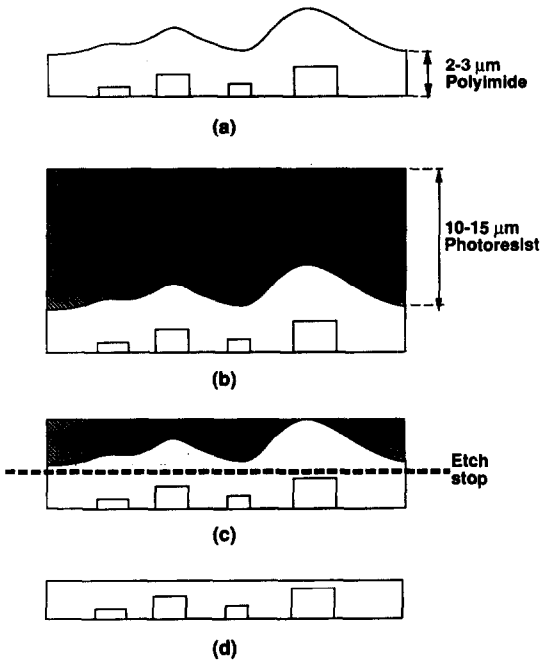


Fig. 3. The sequence of the plasma etch back process: (a) polyimide spin: (b) thick photoresist spin to obtain a planar surface that is independent of the substrate topography; (c) since the etch rate ratio of PR to PI is close to 1, it is possible to carry the etching down to the etch stop point without degrading planarity; (d) final planarized surface.

Initial experiments were carried out with silicon chips that are fabricated by MOSIS, a VLSI foundry that allows merging of different project chips of various sizes on a single wafer. Unfortunately, the limited MOSIS die size can cause problems during the application of the PEB technique. This is due to the "edge bead" that is created on a chip after PI spinning. Edge bead is the accumulation of PI around the periphery of a chip due to the discontinuity of silicon surface. The effect can be very severe for a small chip size such as 5 by 7 mm. DEKTAK scans showed that the PI was several times thicker around the edges of such a chip compared to the regions in the middle. If the III–V film size is close to the chip size, water can be trapped in the center region of a film during bonding due to the concave shape of the PI top surface. Obviously, this could result in blisters and poor film adhesion. Therefore, ELO film size should be chosen in such a way that it only covers the flatter central section of such a Pd/polyimide coated IC chip.

To reduce edge bead, a special aluminium jig was designed in which a chip can be embedded. This way, it is possible to level the surface of a chip with the surrounding aluminum and create a continuous top surface during PI and PR spinning. Although this design helped to reduce the size of the edge bead, it did not eliminate it completely. Other techniques, such as embedding a silicon chip in wax until its surface is level with the surroundings did not prove to be very successful either. As a result, the periphery within 1 mm of each edge of a chip was not planar. For a chip size of 5 by 7 mm, this corresponds to 60% reduction of useful silicon area.

3.1.1. MOSIS chip integration based on plasma etch back: A driver chip was designed to demonstrate GaAs LEDs working with silicon circuits. The chip contains a 4 × 8 array of analog current driver cells whose current can be set between 2 to 20 mA by simply reducing the values of V_{DD_2} and V_{DD_3} (Fig. 4). The input stage consists of 3 inverters that scale up at each stage to minimize the input signal propagation delay. The output stage consist of a very large p-type transistor whose output needs to be connected to the n-side of an GaAs LED. The p-side of the LED is bonded onto a Pd coated substrate that serves as external power supply pad (V_{DD_3}) to the circuit. The chip was designed according to the 2 μm design rules of MOSIS. The maximum peak to valley height of the surface features on the chip was initially 3 μm. In a later design, this was reduced to 1.5 μm by taking careful advantage of the MOSIS design rules to simplify the planarization process. The chip size is 5 by 7 mm. It was planarized by applying the PEB procedure twice. This starts with spinning DuPont 2555 polyimide (PI) at 3500 rpm, and Shipley SP-90190-44 photoresist (PR) at 4000 rpm. In this way, we have a 3 μm thick PI and 7.5 μm thick PR before plasma etching. After the removal of photoresist (a dummy silicon sample spun with PR was used for this purpose), the PI was etched into for an additional micron. The sample went through a second PEB step by simply spinning another layer of 3 μm thick PR. This time, only 0.2 μm of polyimide was etched after the removal of the PR. At the end of the second PEB, there is about a 2 μm thickness of PI covering the surface of the chip. It is important to control the thickness of this layer, as it can cause metal step coverage problems when connecting GaAs LEDs to the silicon circuits. Finally, a 0.2–0.5 μm thick layer of polyimide (diluted DuPont 2555) was spun to further eliminate the micro roughness of the surface after the long etching process. At this point, the sample is planar enough to allow high quality bonding of III–V films. Figure 5 shows all the important steps of the fabrication after planarization. A detailed description of the process is given in Appendix 1. Figure 6 shows a portion of the driver chip with fabricated LEDs connected to silicon circuits. These LEDs are placed in dedicated "circuit free" areas

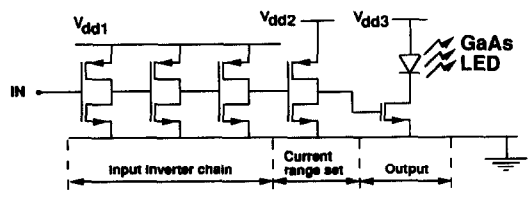


Fig. 4. The schematics of the driver chip to be used with the epitaxial liftoff LEDs.

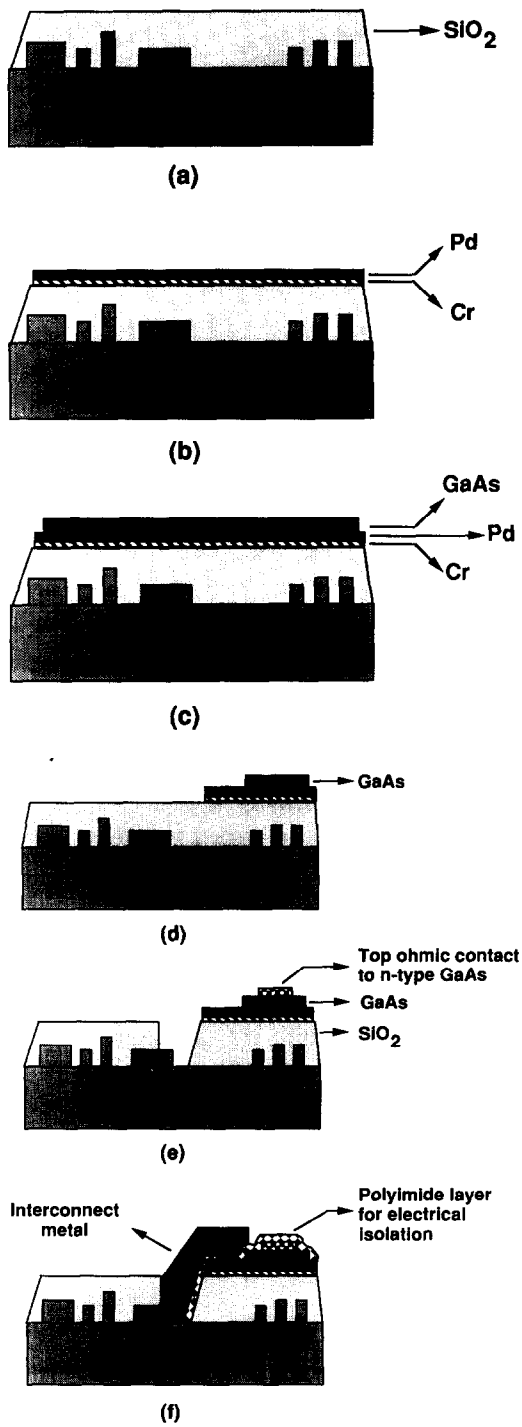


Fig. 5. The sequence of the post-processing steps to fabricate GaAs LEDs: (a) planarized silicon chip; (b) Cr/Pd deposition; (c) GaAs film bonding; (d) patterning of GaAs and underlying metal layers; (e) top n-type ohmic contact metallization followed by contact hole openings for the p-type GaAs to silicon circuit interconnect; (f) polyimide spin for LED sidewall isolation and final metallization.

where planarization is relatively easier. However, our planarization techniques were good enough to allow high quality bonding directly on "circuit areas". Figure 7 shows a picture of such an LED emitting light. It is important to be able to place LEDs right on top of silicon circuits rather than on dedicated circuit-free areas. In this way, considerable real estate can be saved, making this integration technique more favorable for ULSI applications.

3.2. Chemical-mechanical polishing

CMP relies on polishing with a pad and a slurry of colloidal silica abrasive particles (10 nm in diameter) that are suspended in KOH solution. The low cost of polishing makes it very attractive for IC foundries to use as a standard processing step. Some of the IC foundries have already started using it in their multilevel metal processes. Polishing machines with a throughput of 60 wafers/h are commercially available. This process has matured to the point that contractor companies can deliver high quality polished processed wafers for a basic service fee.

During our research, it has been found out that polishing of chip areas is quite straightforward where the maximum valley-to-peak height of surface topography is $<3\,\mu$m. However, the separations between chips, usually called streets, are much more challenging to planarize as the step height from streets to chips is in general 5–7 mm. This is almost twice the maximum step size one encounters within a typical chip area. One obvious solution is to modify the processing masks so that street regions are level with the remainder of the chip area. Unfortunately, one seldomly has control over such a foundry process. In addition, streets are preferably left blank for proper dicing purposes. One could solve the problem by neglecting street areas and perform ELO only on planarized chip areas. In our approach, we have planarized the entire wafer including streets. This way, it is possible to do large area liftoff on silicon wafers regardless of their topography.

A post processing step was applied to fabricated foundry wafers to fill up the street regions. For this purpose, a Phosphorus Silica Glass (PSG) layer of 5–7 μm was deposited on wafers using atmospheric CVD at 450°C. Phosphorus composition of the PSG was kept very high to prevent the glass films from cracking. This high phosphorus glass film was sandwiched between two layers of undoped silica film, of 0.5 μm thickness, to prevent moisture related problems.

The samples were sent to various companies to carry out the polishing process[14]. No Newton rings were observed on the wafers after polishing indicating the quality and uniformity of the process. As in the case of polyimide, it is desirable to remove as much SiO_2 as possible. In this way, the vertical height difference between GaAs LEDs and Si circuits is minimized.

3.2.1. Large area liftoff on 5″ polished Si device wafers: The initial experiments were done with process 5″ reject wafers obtained from Si foundries. The

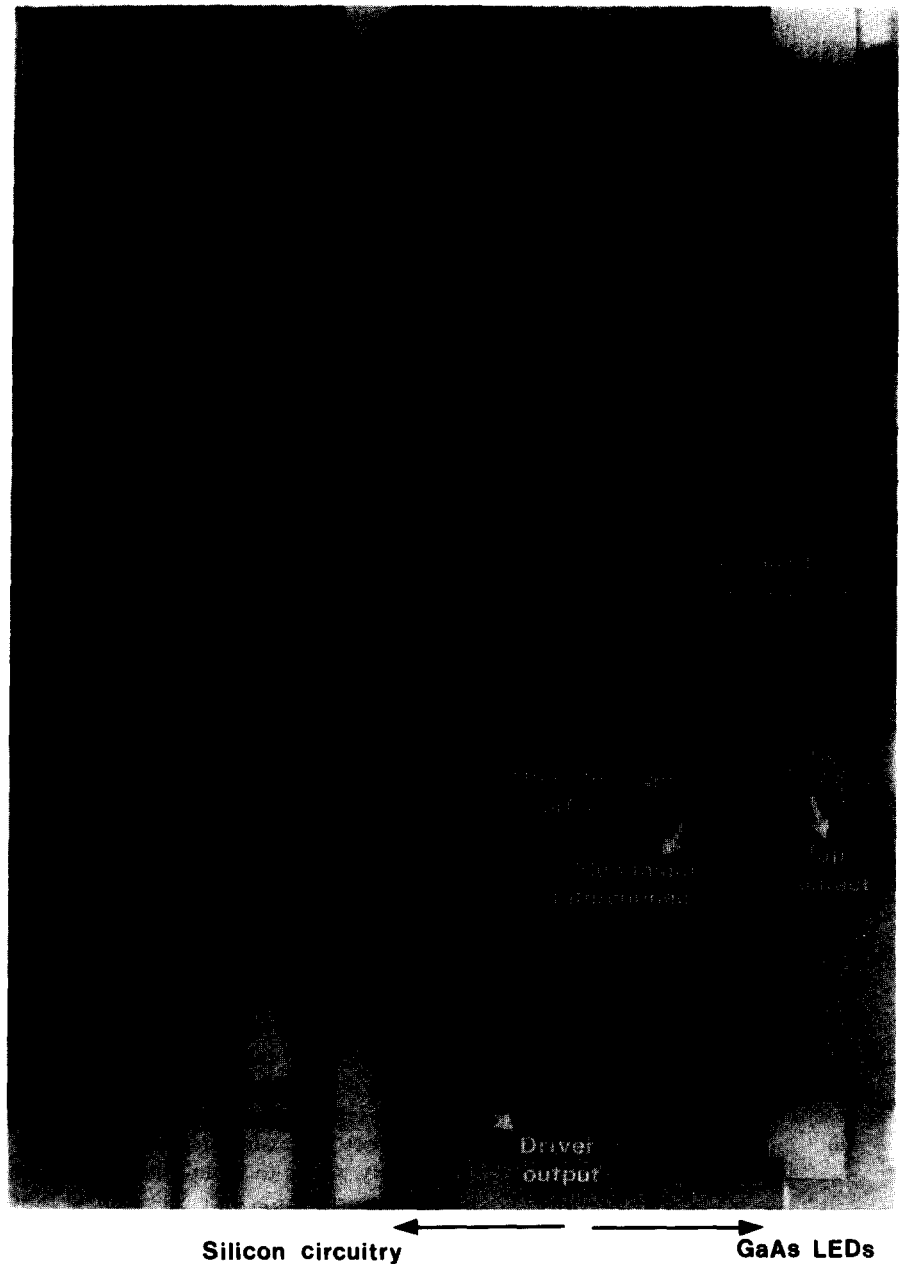
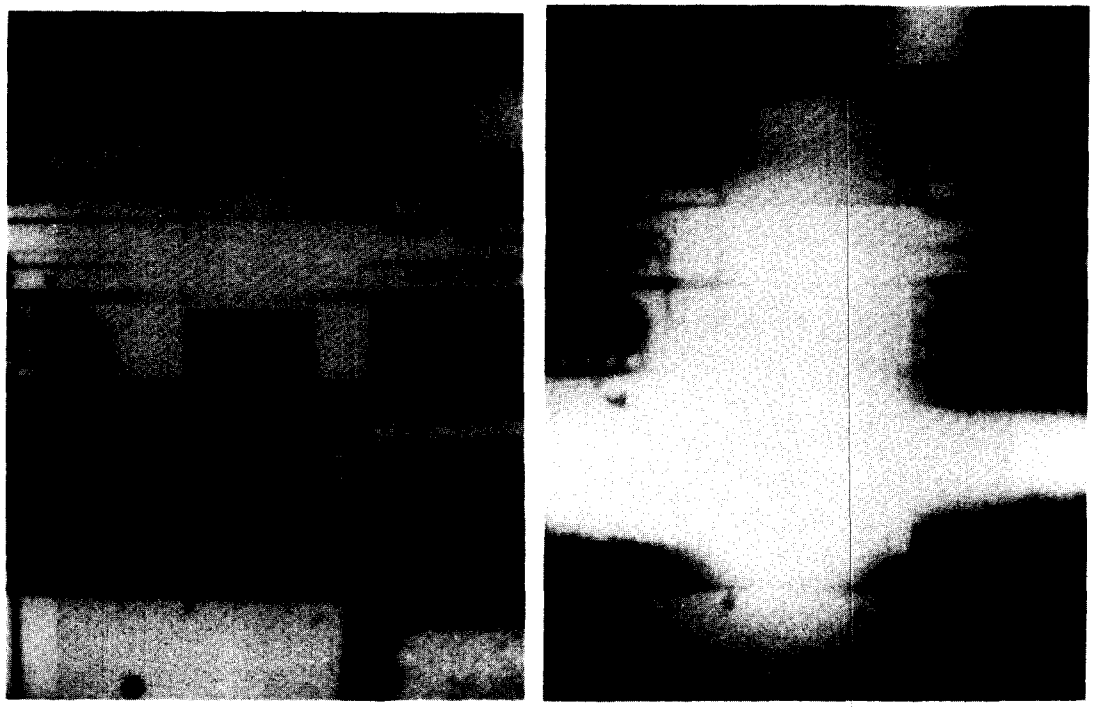


Fig. 6. Micrograph showing a row of LEDs connected to silicon driver circuits. Here LEDs are placed in dedicated regions where there were no silicon circuits.

size of the wafers was dictated by the handling capability of standard commercial polishing equipment. The wafers were coated with PSG glass and sent out to various polishing companies. After polishing, the glass was coated with 0.02 μm of Cr and 0.05 μm of Pd by evaporation. At this point, the wafers are ready for the direct bonding of the ELO films.

We prepared epi-GaAs samples that were 50 mm long and 10 mm wide by cleavage. They were then covered with Apiezon W wax. After baking the wax at 160°C for 15 min, streets were patterned into the wax to reduce the undercutting time of the AlAs (Fig. 8). The streets in the wax were cut with a hot blade to expose the top layer of the III–V heterostructure. The pressure of the hot blade is adjusted in such a way that it barely touches the top layer of the wafer and avoids damaging it. The sample is then taken to an oxygen plasma for about an hour to clear the streets entirely. Using the patterned wax as a mask, a wet etching step is carried out to expose the AlAs layer. The stripes are stitched together with an acid resistant tape to prevent them from lifting off individually. At this point the sample is ready to go into 10%



(a) (b)

Fig. 7. (a) Micrograph of an LED that has been placed directly right above silicon micro-circuitry. (b) The same LED emitting light.

HF solution for liftoff. Figure 9 is the photograph of a 5″ planarized silicon wafer with a large area liftoff film bonded on top. This particular sample did not have patterned stripes and was lifted off as a whole after a long etching time (approx. 48 h). Film areas which are free of blisters and cracks after bonding are strong enough to withstand rigorous processing steps such as photoresist removal with cotton swaps. However, 5–10 blisters, 0.25 mm in diameter, have been noticed on some 10 by 50 mm samples. There are at least two possible sources of these imperfections: the quality of polished surfaces and the quality of the grown epi-films. As for the quality of polished substrates, there are some particles on the oxide after polishing. They could be dust particles present in the environment or oxide flakes that come off during polishing process. We have made considerable progress regarding this problem after gaining more

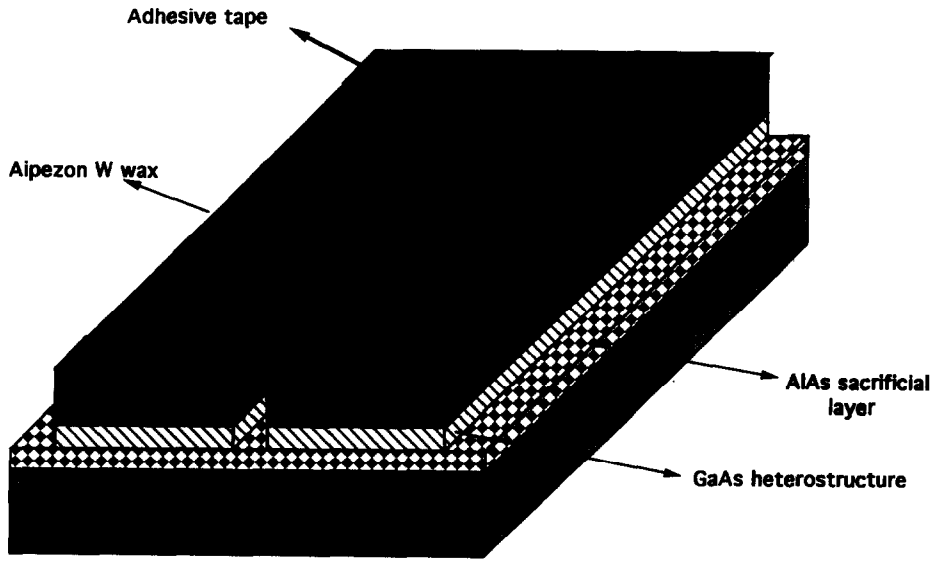


Fig. 8. The illustration of the sample after wax patterning. HF can attack the sacrificial AlAs layer through the streets which have been patterned in the wax.

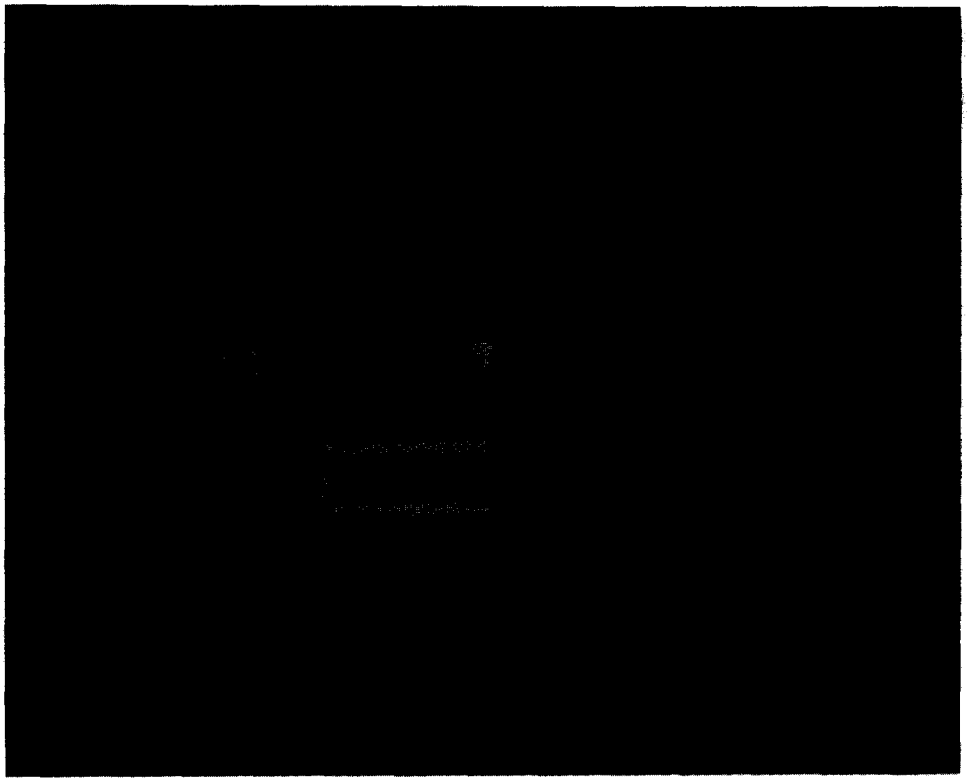


Fig. 9. A photograph of a 5″ silicon wafer after bonding large area liftoff films. The films can be further processed after this stage to finish the fabrication of GaAs devices.

experience in polishing. At the present time the second problem, the quality of the GaAs epi-material growth, is also challenging. Epitaxial liftoff reveals and makes conspicuous every pinhole, pit or other defect which had been present in the original substrate. Materials from five different epi-GaAs vendors have been studied for liftoff experiments. Except for one vendor, all of them showed similar imperfections. These imperfections will dissappear with improved substrate preparation conditions. In the worst case, they will be a yield limiting factor. Areas as large as 4 cm^2 with virtually no defects have been successfully bonded onto Pd coated silicon substrates.

3.3. Electrical measurements

Four wafers grown by different vendors were used to evaluate the electrical performance of devices after liftoff. Two square pieces (1 × 1 cm) were cut from the center region of each wafer. One of these pieces was saved for ELO whereas the other one was saved for a conventional LED fabrication. At the end, there were a total of eight samples with four of them lifted off and bonded on silicon substrates. All the samples went through similar processing steps excluding the metallization for the p-side GaAs ohmic contact. In the case of the liftoff samples, the palladium bond is also used as the bottom contact to the p-side GaAs reducing the number of steps required for LED fabrication [Fig. 10(a)]. An extra etching and metallization step had to be included to realize the p-side contact of the conventional LEDs [Fig. 10(b)].

Figure 11 shows typical I–V characteristics of a lifted-off, vertically injected LED and a laterally

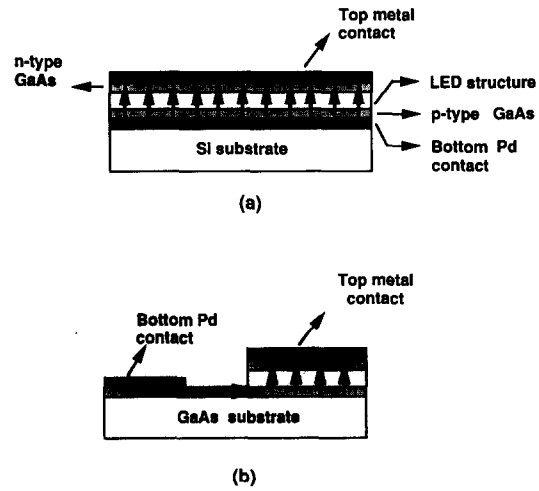


Fig. 10. The liftoff LEDs do not require a p-type metallization step (a). Electrical injection to the same LED structures grown on semi-insulating substrates requires additional mesa etching (b). Clearly the resistance of the vertically injected LEDs, (a), is lower than for the laterally injected LEDs, (b).

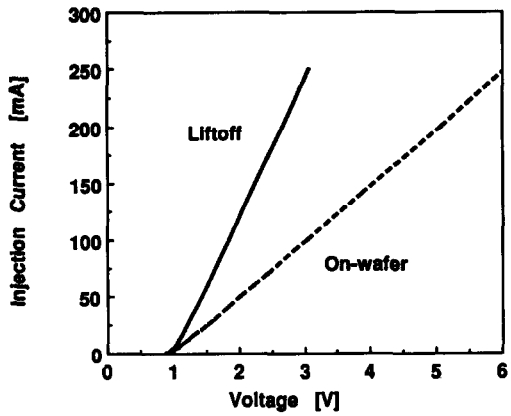


Fig. 11. Typical I–V characteristics of a liftoff LED and on-wafer LED, as described in Fig. 10.

injected, on wafer LED. The liftoff LED, have a lower series resistance compared to the on-wafer LEDs. (Typically, 8 vs 20 Ω). This is due to the shorter current path of the liftoff LEDs as can be seen from Fig. 10(a) and (b). The liftoff LEDs that coincide with obvious visual damages (dislocations, cracks, blisters) have poor I–V characteristics or they do not function at all. However, those areas account for less than 0.1% of the total area. One of the ELO samples was fully tested and 649 LEDs functioned well, confirming our high yield expectations for the process.

4. CONCLUSIONS AND FUTURE GOALS

ELO has proven itself as a viable approach to integrate Si and GaAs. There are some practical considerations that still need to be improved to make ELO as routine a technique as flip chip bonding. For this purpose, a set of handling tools are being designed that would make ELO possible even in the hands of an unskilled person after a brief training.

Yield will be the most important issue in determining whether ELO will be widely used or not. There are two important factors affecting yield: The planarity of the substrates to which the film will be bonded, and the foundry grown quality of ELO films. The latter is the more crucial requirement. We are currently collaborating with several foundries to improve the quality of epi-grown GaAs films.

Two different planarization techniques have been shown to be successful to carry out the direct bonding process: plasma etch back and chemical–mechanical polishing. CMP seems to be the more promising approach due to its cost effectiveness for mass production. A 32 × 32 array demonstration using CMP is being designed. This array will include Si detectors and Si logic circuitry integrated with GaAs LEDs.

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APPENDIX 1

Sequence for GaAs/Si integration process after planarization:

1. Evaporation of 0.025 μm thick Cr followed by 0.05 μm thick Pd. Cr serves as an adhesive layer between the oxide and Pd layer, since the adhesion of Pd directly on oxide is poor.
2. Direct bonding of epi-liftoff film to the chip surface. The sample was pressed under a weight of 15 g/mm^2 for 24 h. The p-side of the film was pressed against the Pd substrate which makes a good ohmic contact to p-type GaAs.
3. Mask 1, patterning of the GaAs film to make individual LEDs. In this case, LEDs are 100 × 100 μm squares.
4. Mask 2, patterning of the Pd layer to electrically isolate each LED. Each Pd island is a rectangle of 200 × 120 μm. GaAs islands are sitting on these Pd islands. The unoccupied part of the island serves as the bottom contact (p-type contact). This is also a contact pad for the V_{DD_1} of the driver circuit.
5. Polyimide spin (0.5 μm thick) to isolate the sidewalls of GaAs LEDs.
6. Mask 3, Contact hole opening in the top PI layer to make contact to the bottom and top layers of the LED structure.
7. Mask 4, Ohmic contact to n-type GaAs. A sequency of Pd/Ge/AuGe/Au with 0.02/0.02/0.03/0.08 μm thicknesses were evaporated for this purpose.
8. Mask 5, contact openings in the planarized polyimide layer to allow the electrical connection of GaAs LEDs to silicon circuits. As mentioned above, the total thickness of this PI layer is 2.5 μm.
9. 2.5 μm thick Al evaporation.
10. Mask 6, pattern the aluminium.