INTEGRATION OF GaAs LEDs WITH SILICON CIRCUITS

BY EPITAXIAL LIFTOFF

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ABSTRACT

Epitaxial liftoff has emerged as a viable technique to integrate GaAs with silicon. The technique relies on the separation of a thin epi-GaAs film from its substrate followed by direct bonding of the thin film to a silicon substrate. The silicon substrate has to meet certain planarity and smoothness conditions in order to obtain high quality bonding. Unfortunately, processed silicon IC chips do not satisfy these conditions. In this paper, we report on the results of two different planarization techniques, plasma etch back and chemical mechanical polishing, to integrate GaAs LEDs with silicon circuits using epitaxial liftoff. A 4 by 8 array of GaAs LEDs have been integrated with silicon driver circuits using plasma etch back. We also have lifted off areas as large as 500 mm^2 and bonded them on five inch device wafers by chemical mechanical polishing.

1. INTRODUCTION

The three dimensional nature of optics makes it valuable for parallel processing of massive data. In order to out-perform purely electronic systems, very large number of optoelectronic processors are needed. In such a system, each processor has light sources and detectors to communicate with other processors. Although the complexity of circuitry depends very much on the type of problem, most of the proposed architectures require several hundred to several thousand transistors in each processor. Silicon is the only technology today that can deliver such a large array of processors in a plane with a finite yield. Unfortunately, efficient light sources can not be made from silicon as it is an indirect bandgap material. Thus, a technique needs to be developed to integrate silicon with other light emitting materials such as GaAs. This technique should be able to deliver high performance components with acceptable yields.

In this paper, we report an new technique, Epitaxial Liftoff (ELO), that can be regarded as a semi-monolithic approach. With this technique, a thin film of GaAs

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is separated from its substrate and then transferred to the top of silicon circuits. This way, it is possible to utilize three dimensional OEICs where the top layer contains light sources. These light sources are vertically interconnected to underlying silicon circuits. The ease of application of ELO to Si/GaAs and high yields obtained with this technique can make it a possible alternative to flip-chip bonding.

2. EPITAXIAL LIFT-OFF

The details of ELO process can be found in references 1-3. The process is illustrated in Figure 1. There are two important steps in the process. The first one is the removal of a thin GaAs film from a substrate and the second step is the transfer of this film onto a different substrate. The first step relies on the fact that the etch rate of AlAs is much faster than $GaAl_xAs_{1-x}$ in HF. Therefore, a sacrificial layer of AlAs is grown between the GaAs heterostructure and its substrate. A thick Apiezon W wax on the top of the heterostructure gives the thin film some mechanical strength and handling capability after detachment from its substrate. Excess wax is removed from sample edges by grinding or by simply cleaning it with trichloroethylene to expose AlAs sacrificial layer to 10% HF etching solution. The sample is then left for several hours in this dilute HF solution to remove the sacrificial layer. The thin film separates from its substrate upon removal of the AlAs sacrificial layer. Following the further dilution of the HF acid with DI water, the film is picked up with a vacuum tweezer and transferred on to a different substrate which happens to be a processed silicon wafer in this case.

The second step is the bonding of III-V thin films onto silicon substrates. This is the more critical step as the quality of adhesion affects yield directly. The nature of the bonding mechanism depends on the type of substrate surface the film has been transferred to. It has been attributed to Van der Waals forces in the case of SiO_2 and polyimide substrates. Unfortunately, the adhesion can be incomplete due to the weak nature of these forces. This partial adhesion can be a much more severe problem if the film has to be processed after bonding. During post-fabrication, the film would be more vulnerable to steps such as blow drying, photoresist removal, etc.

A much better bonding can be achieved if the substrate is covered with Pd [3]. GaAs alloys with Pd even at room temperature, forming the intermetallic compound Pd_4GaAs. The result is an excellent bond that survives the "scotch tape test". The bond strengthens rapidly if samples are annealed at 200 °C in N_2 ambient for an hour. It has also been found out that the metallurgical bond

becomes stronger if samples are left under ambient conditions for several days. Besides being the perfect glue, Pd offers some additional important advantages: It makes a good ohmic contact to p-type GaAs. This makes it possible to use Pd coated substrate as the bottom contact to GaAs devices. Being a metal, Pd can also be used as a heat sink which is essential for proper operation of active GaAs devices.

The III-V films can be pre-processed or post-processed relative to the bonding step. In the pre-processed case, fully fabricated devices exist in the film before liftoff and the thin film has to be aligned with respect to the features on substrate it will be bonded to. In the post-processed case, the unprocessed film is bonded to a substrate requiring no precise alignment. All the device fabrication is done after bonding. The disadvantage of this technique is that it demands strong adhesion. However, this has not been a problem with the strong bond obtained from Pd/GaAs interface. Therefore, the work in this paper is based on post-processing of devices after bonding to a Pd coated substrate. This way, the problem of aligning existing devices with respect to circuit features in the silicon substrate has been eliminated.

A Pd coated substrate is not sufficient to obtain good adhesion of GaAs films. The substrate has to meet certain smoothness and planarity conditions at the same time. Thin films can stretch over steps that are within the "three degree condition" [4]. That is, the slope of the surface should not exceed three degrees from normal at any given point on a substrate. For example, this corresponds to a height difference of 0.05 μm between the points that are separated from each other by 10 μm. This "three degree condition" makes the requirements on global planarization less strict as long as local planarity is satisfied across a wafer. A typical silicon chip has up to 3 μm steps with a largely varying spatial frequency. Therefore, it is essential to develop a general planarization technique that is independent of the topography of underlying layers. The substrate smoothness and planarization is so important that the ELO yield is limited to a great extent by the quality of finished surfaces. The next section will review ELO results obtained on surfaces planarized using different techniques.

3. ELO ON PLANARIZED SURFACES

Planarization is an important issue in multilevel metal processes where the insulator thickness between two metal layers has to be controlled with great accuracy to satisfy requirements related to Ultra Large Scaled Integration (ULSI). The limited depth of focus (DOF) of exposure tools for optical lithography has been the major driving force behind planarization requirements. DOF requirements are a function of exposure wavelength and lithographic resolution.

For example, DOF is limited to 0.38 μm at 240 nm for a minimum feature size of 0.3 μm. [5]. This obviously makes the planarization of interlevel dielectrics a very important part of the entire process. Therefore, a large variety of techniques have been developed. Some of these techniques are becoming a standard step in the fabrication of ICs and are widely used by most of the major foundries. Two different planarization techniques were chosen to demonstrate ELO: The first one is Plasma Etch Back (PEB) and it was used for small size silicon chips (5 mm by 7 mm for example). The second technique is Chemical Mechanical Polishing (CMP) and it is generally restricted to large wafers (4 " and larger). This is due to the fact that all the commercial polishing machines are designed for large size wafers to match standard IC foundry sizes. In this section, PEB and CMP will be briefly reviewed.

3.1. Plasma Etch Back

In PEB, the sample is first spun with 3-4 μm thick polyimide (PI). It is then coated with a very thick photoresist (PR) layer so that the final surface is almost planar independent of the silicon chip topography (Figure 2). Although one can initially start with a very thick layer of PI, severe cracks were seen after exposing PI to plasma for a long time. A combination of PI and PR tends to reduce these cracks, if not completely eliminate them. The sample is then put in an O_2 plasma and etched down all the way to the photoresist/polyimide interface. As the etch ratio of photoresist and polyimide can be made very close to each other by adjusting the etching conditions (1 : 0.95 in our experiments), one would eventually end up with a planar surface if the etching is carried out until the photoresist has been removed entirely. This technique can be applied as many times as necessary until the desired planarity has been reached. Very smooth surfaces (100 Å surface roughness over a 3 μm distance) have been achieved using this technique. DEKTAK measurements and visual inspections with a microscope will determine whether the surface is planar enough to allow high quality film bonding. A very good indication of desired planarity can be obtained by visual inspection after Pd evaporation onto planarized surfaces. Basically, at this stage samples should like a flat mirror and one should not be able to see any features of the silicon circuitry under the Pd thin film coating.

A driver chip was designed to demonstrate GaAs LEDs working with silicon circuits. The chip size is 5 mm by 7 mm. It was planarized by applying the PEB technique twice. The process starts with spinning DuPont 2555 polyimide (PI) at 3500 rpm and Shipley XP-90190-44 photoresist (PR) at 4000 rpm. This way, we have a 3 μm thick PI and 7.5 μm thick PR before plasma etching. After the removal of photoresist (a monitor silicon sample spun with PR was used for this purpose), the PI was etched into for an additional micron. The sample went

through a second PEB step by simply spinning another layer of 3 μm thick PR. This time, only 2000 Å of polyimide was etched after the removal of the PR. At the end of the second PEB, there is about a 2 μm thickness of PI covering the surface of the chip. It is important to control the thickness of this layer, as it can cause metal step coverage problems when connecting GaAs LEDs to the silicon circuits. Finally, a 0.2-0.5 μm thick layer of polyimide (diluted DuPont 2555) was spun to further eliminate the micro roughness of the surface after the long etching process. At this point, the sample is planar enough to allow high quality bonding of III-V films. Figure 3 shows all the important steps of the fabrication after planarization. Figure 4 shows a portion of the driver chip with fabricated LEDs connected to silicon circuits.

3.2. Chemical Mechanical Polishing

CMP relies on polishing with a pad and a slurry of colloidal silica abrasive particles that are suspended in KOH solution. The low cost of polishing makes it very attractive for IC foundries to use as a standard processing step. Some of the IC foundries have already started using it in their multilevel metal processes. Polishing machines with a throughput of 60 wafers/h are commercially available. This process has matured to the point that contractor companies can deliver high quality polished processed wafers for a basic service fee.

During our research, it has been found out that polishing of chip areas is quite straightforward where the maximum valley-to-peak height of surface topography is < 3 μm. However, the separations between chips, usually called streets, are much more challenging to planarize as the step height from streets to chips is in general 5-7 μm. This is almost twice the maximum step size of one encounters within a typical chip area. One obvious solution is to modify the processing masks so that street regions are level with the remainder of the chip area. Unfortunately, one seldomly has control over such a foundry process. In addition, streets are preferably left blank for proper dicing purposes. One could solve the problem by neglecting street areas and perform ELO only on planarized chip areas. In our approach, we have planarized the entire wafer including streets. This way, it is possible to do large area liftoff on silicon wafers regardless of their topography.

A post processing step was applied to fabricated foundry wafers to fill up the street regions. For this purpose, a Phosphorus Silica Glass (PSG) layer of 5-7 μm was deposited on wafers using atmospheric CVD at 450 °C. Phosphorus composition of the PSG was kept very high to prevent the glass films from cracking. This high phosphorus film was sandwiched between two layers of undoped silica film, of 0.5 μm thickness, to prevent moisture related problems.

The samples were sent to various companies to carry out the polishing process [6]. No Newton rings were observed on the wafers after polishing indicating the quality and uniformity of the process. As in the case of polyimide, it is desirable to remove as much SiO_2 as possible. In this way, the vertical height difference between GaAs LEDs and Si circuits is minimized.

The initial experiments were done with processed 5-inch reject wafers obtained from Si foundries. The size of the wafers was dictated by the handling capability of standard commercial polishing equipment. The wafers were coated with PSG glass and sent out to various polishing companies. After polishing, the glass was coated with 200 Å of Cr and 500 Å of Pd by evaporation. At this point, the wafers are ready for the direct bonding of the ELO films. Figure 5 is the photograph of a 5 inch planarized silicon wafer with large area lifted-off film bonded on the top. Film areas which are free of blisters and cracks after bonding are strong enough to withstand rigorous processing steps such as photoresist removal with cotton swaps. However, 5-10 blisters, 0.25 mm in diameter, have been noticed on some 10 mm by 50 mm samples. There are at least two possible sources of these imperfections: the quality of polished surfaces and the quality of the grown epi films. As for the quality of polished substrates, there are some particles on the oxide after polishing. They could be dust particles present in the environment or oxide flakes that come off during polishing process. We have made considerable progress regarding this problem after gaining more experience in polishing. At the present time the second problem, the quality of the GaAs epi-material growth, is also challenging. Epitaxial liftoff reveals and makes conspicuous every pinhole, pit or other defect which had been present in the original substrate. Materials from five different epi-GaAs vendors have been studied for liftoff experiments. Except for one vendor, all of them showed similar imperfections. These imperfections will disappear with improved substrate preparation conditions. In the worst case, they will be a yield limiting factor. Areas as large as 4 cm^2 with virtually no defects have been successfully bonded onto Pd-coated silicon substrates.

4. CONCLUSIONS

ELO has proven itself as a viable approach to integrate Si and GaAs. There are some practical considerations that still need to be improved to make ELO as routine a technique as flip chip bonding. For this purpose, a set of handling tools are being designed that would make ELO possible even in the hands of an unskilled person after a brief training.

Yield will be the most important issue in determining whether ELO will be widely used or not. There are two important factors affecting yield: The planarity of the

substrates to which the film will be bonded, and the foundry grown quality of ELO films. The latter is the more crucial requirement. We are currently collaborating with several foundries to improve the quality of epi-grown GaAs films.

Two different planarization techniques have been shown to be successful to carry out the direct bonding process: plasma etch back and chemical mechanical polishing. CMP seems to be the more promising approach duo to its cost effectiveness for mass production. A 32 x 32 array demonstration using CMP is being designed. This array will include Si detectors and Si logic circuitry integrated with GaAs LEDs.

5. REFERENCES

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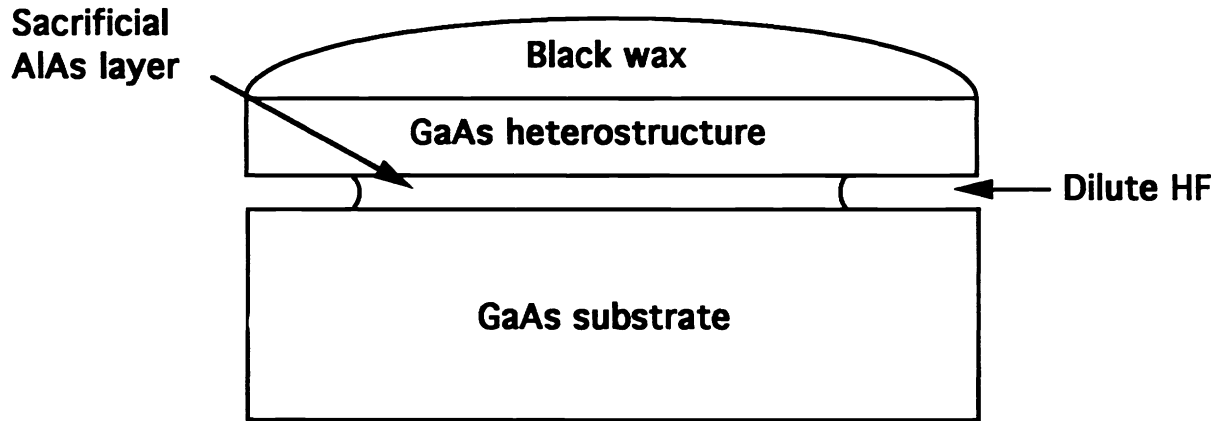


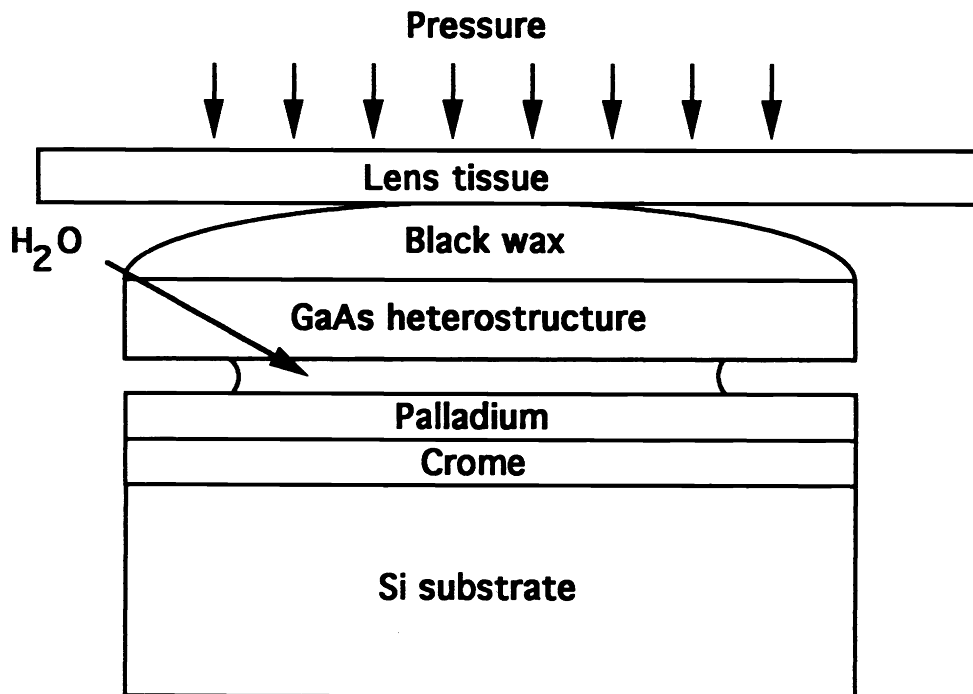


Figure 1. The illustration of ELO process a) Separation of thin film from its substrate b) Bonding of the film onto another substrate that is covered with Pd.

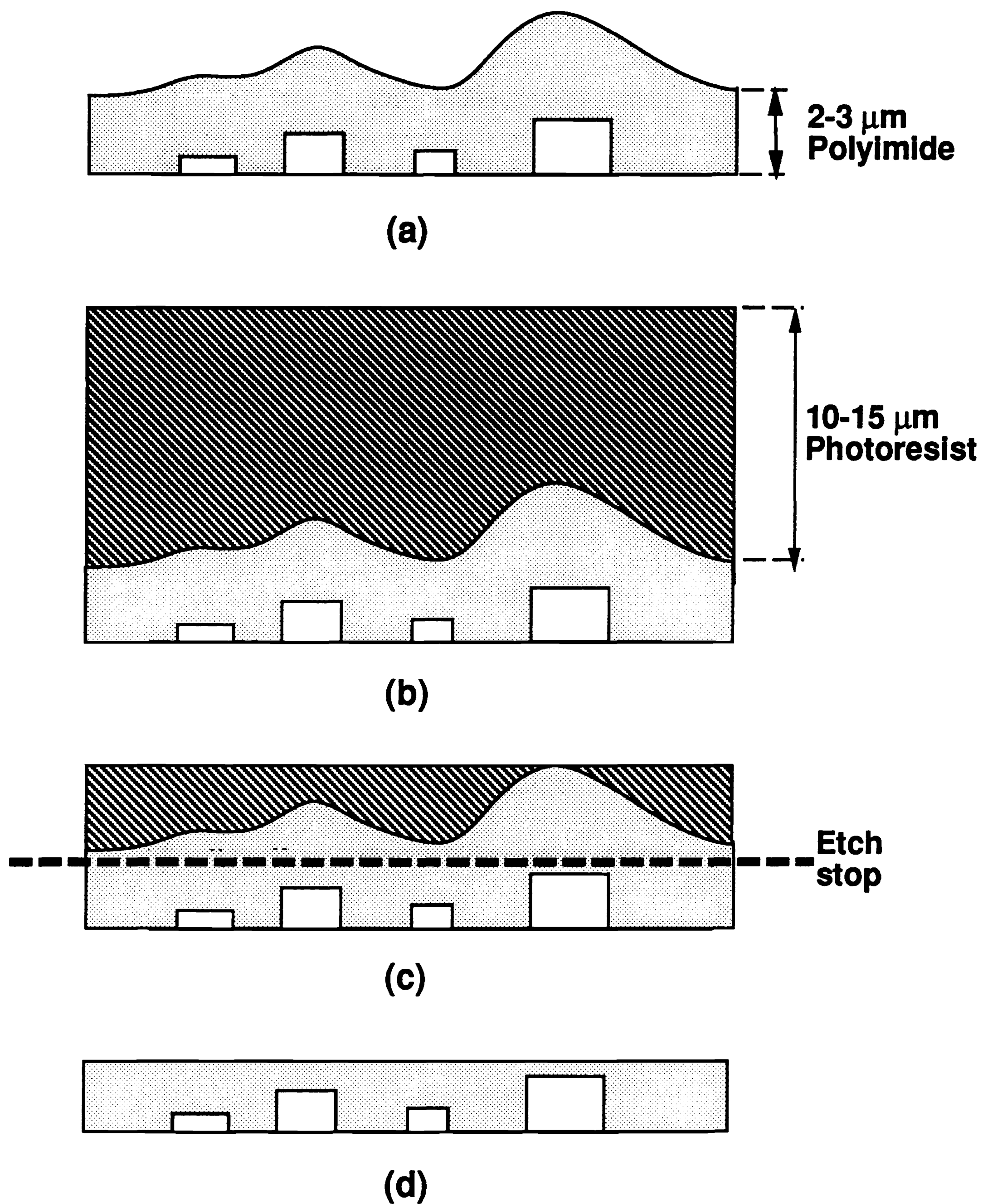
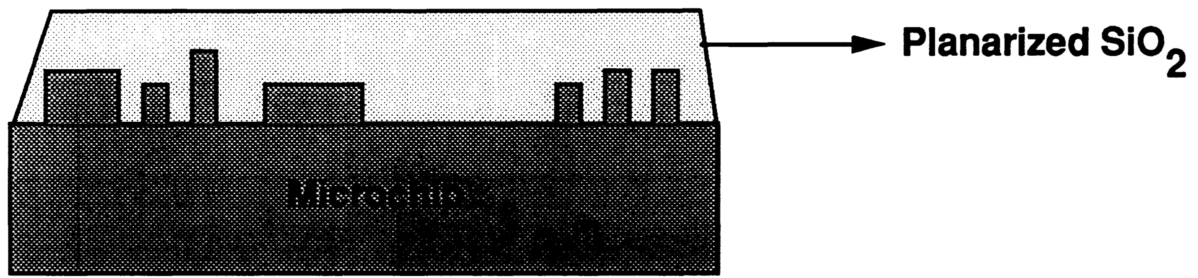
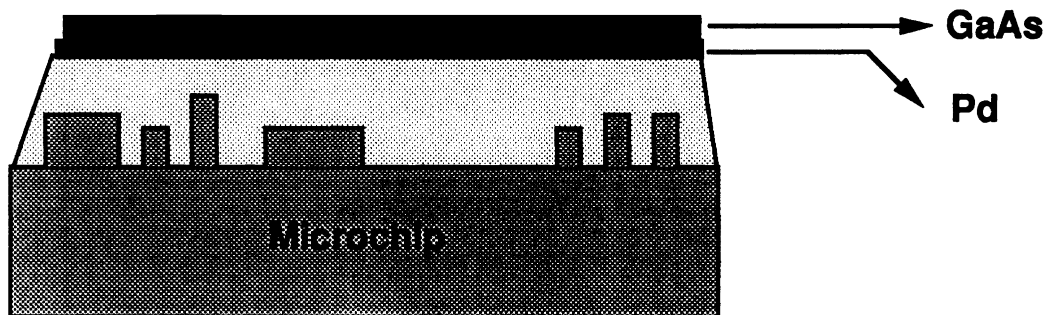


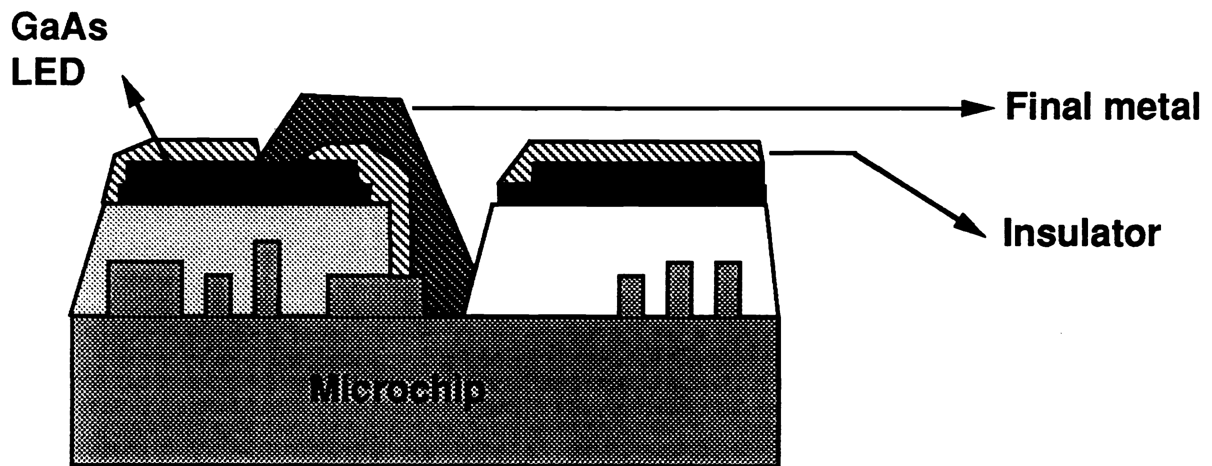
Figure 2. The sequence of Plasma Etch Back a) Polyimide spin b) Thick photoresist spin to obtain a planar surface that is independent of surface topography
c) Since the etch rate ratio of PI to PR is close 1, it is possible to carry out the etching down to the stop point without degrading planarity
d) Final planarized surface



(a)



(b)



(c)

Figure 3. The sequence of the post-processing steps to fabricate GaAs LEDs
a) Planarization of the Si chip b) Pd evaporation followed by GaAs film bonding
c) Contact hole opening and metallization

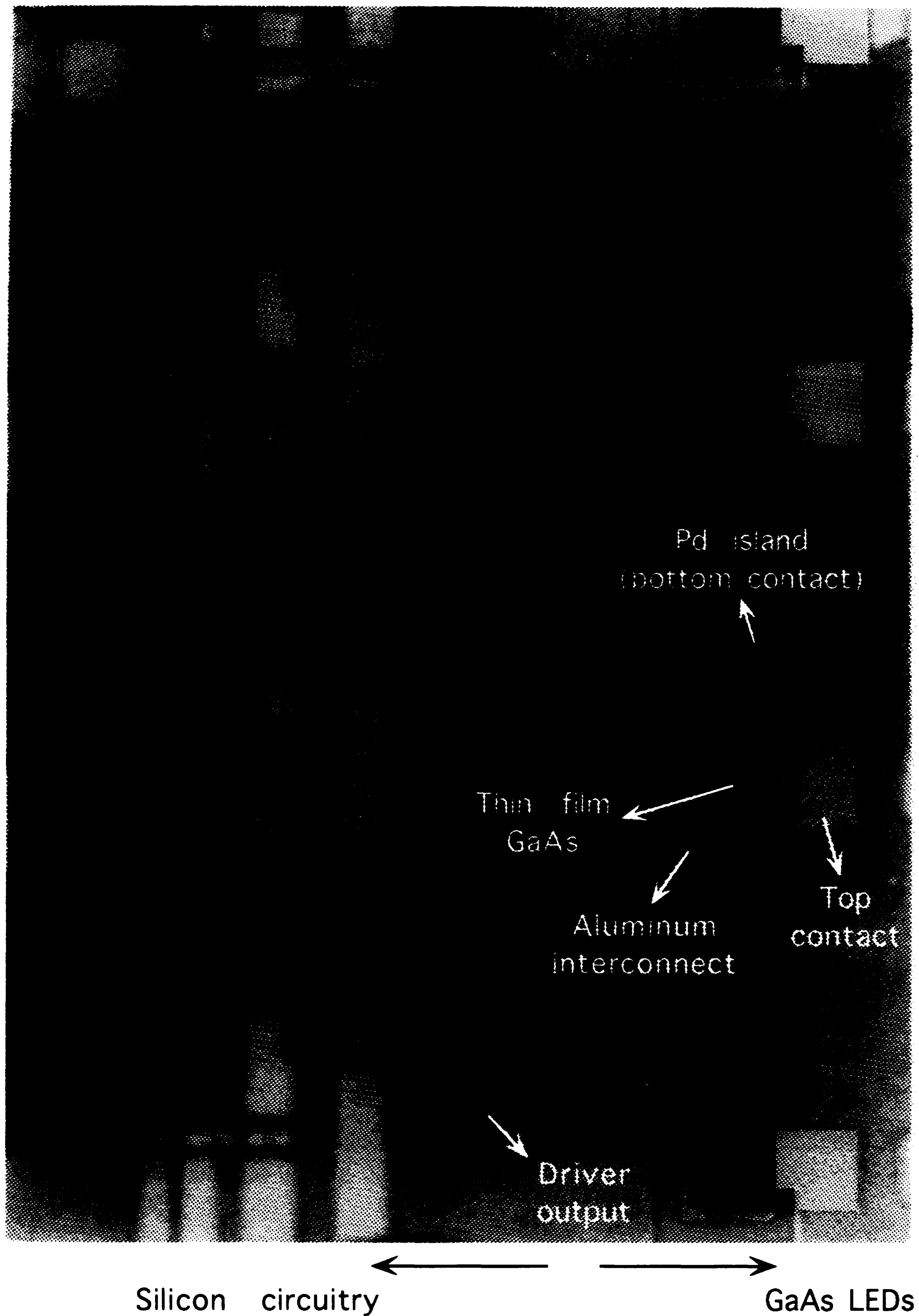


Figure 4. Micrograph showing a row of LEDs connected to silicon driver circuits. Here LEDs are placed in dedicated regions where there were no silicon circuits.

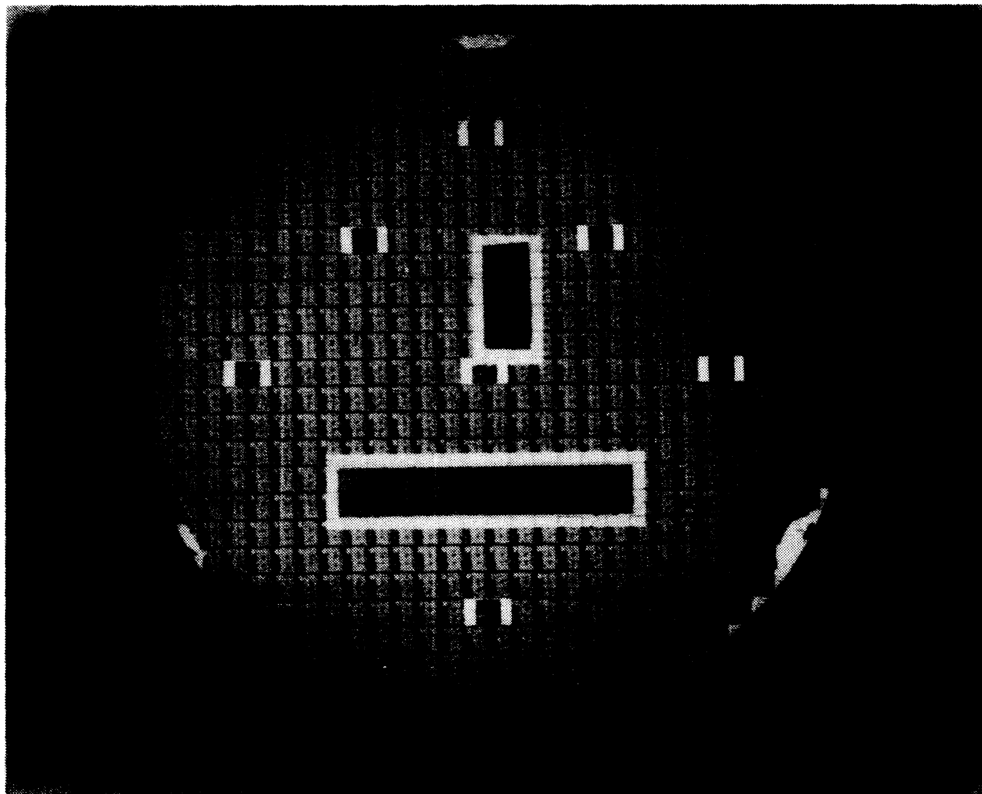


Figure 5. The photograph of a 5-inch silicon wafer with fabricated circuits after bonding large area lift-off films. The films can be further processed to finish the fabrication of GaAs LEDs.