Van der Waals bonding of GaAs on Pd leads to a permanent, solid-phase-topotaxial, metallurgical bond

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Various forms of wafer bonding have now emerged as a serious competitor to heteroepitaxy for optoelectronic integration of dissimilar semiconductor materials. Among the types of wafer bonding, perhaps the most flexible is that which employs free-standing III-V films as created by epitaxial liftoff. For some purposes, weak Van der Waals forces provide an adequate bond between the native oxides of the III-V film and its new substrate. If the substrate is coated by palladium however, a low temperature solid-phase-topotaxial reaction occurs, producing oriented Pd₄GaAs under the GaAs film. In effect, the topotaxy comes about through mechanical contact alone. The resulting metallic bond is an ohmic contact, a thermal contact and a robust, permanent, adherent contact.

Wafer bonding has now emerged¹ as a direct approach for the integration of dissimilar semiconductor and optoelectronic materials. In this respect, it is quite competitive with other approaches, such as heteroepitaxial² crystal growth.

The central problem in wafer bonding is how to merge two rigid, three-dimensional, objects, namely the two semiconductor wafers. Generally, the wafers do not perfectly conform to one another, topographically, on the scale of atomic dimensions. Ridges and valleys on the mating surfaces leave crevices and openings which prevent adhesion. This problem is partly ameliorated by a high quality planar optical polish on the surfaces, leading to a form of bonding which has been called³ “optical contacting.” More generally the problem of crevices has been dealt with by mechanical pressure and heat: Mechanical pressure increases the area of contact and reduces the size of crevices. Furthermore, high temperatures allow sintering which further fills in the crevices.

A number of specific wafer-bonding material combinations have been worked out:

1) GaAs wafers have been fusion bonded to Corning 7056 glass near the glass transition temperature. The mounted GaAs wafer is then selectively chemically thinned by means of an etch-stop layer to make photomultiplier cathodes.⁴

2) Silicon has been bonded⁵ to oxidized silicon wafers for the purpose of making silicon-on-insulator (SOI) films. Etch stops allow total substrate etching to terminate at the desired epitaxial layer. Temperatures as high as 1400 °C are required for the best possible interfacial adhesion.

3) Under uniaxial pressure, InP wafers have been bonded⁶ to GaAs in a hydrogen atmosphere at temperatures ~ 600 °C which allow chemical vapor transport to fill in the crevices.

4) Likewise III-V wafers, pressed against silicon wafers have been bonded under ultraclean conditions.⁷ At temperatures of only ≤150 °C, Van der Waals bonding and/or hydrogen bonding provide adequate adhesion.

From these examples, we see that wafer bonding has relied on full thickness semiconductor wafers which are later thinned by total substrate etching to make a useful semiconducting thin film. Pressure and temperature have been used to fill in the crevices between the wafers.

Recently, some new thin film bonding approaches were developed. Handling techniques have now been perfected to separate thin epitaxial films from their original growth substrates and to bond them directly onto foreign substrates. The separation process,⁸ called epitaxial liftoff (ELO), relies on an ultrathin AlAs sacrificial layer. Extremely selective etching (≥ 10⁵) of AlAs in dilute hydrofluoric acid allows crack-free GaAs epitaxial films (supported by wax) to be undercut and lifted off a reusable GaAs substrate.

Bonding a thin semiconductor film has a special advantage compared to bonding a thick wafer. The mechanical flexibility of the thin film allows it to conformally conform to the surface undulations of the target substrate. This minimizes the sintering and high pressure required for filling in the crevices. The resulting bond has been called Van der Waals bond⁹ due to the presumed role of such intermolecular forces. The main advantage of thin film Van der Waals bonding is that the mechanical flexibility of the thin film allows bonding to nonplanar substrates, such as fully processed silicon wafers from a foundry. This presents a speedy path toward commercialization of GaAs/Si technology.

Cross-sectional transmission electron microscope (TEM) analysis⁸ of thin film Van der Waals bonding directly onto semiconducting and insulating substrates (Si, III-V’s, SiO₂, LiNbO₃, etc.) showed that the bonding layer consisted of 20–100 Å of native oxides. Clearly, there are reasons for also bonding directly onto a metal-coated substrate as well. A buried metal layer can have high thermal conductivity and can be used as a buried ground plane or as a Schottky barrier or ohmic contact.

Palladium has special advantages for these purposes. Pd is the only metal which readily reacts with both ele-
In the "Van der Waals" bonding process a thin epitaxial film is married to a foreign substrate. After epitaxial liftoff by selective etching, the film is supported by Apiezon W, a wax-like material. The surface tension of de-ionized water acts initially to pull the film down onto the substrate. Then pressure must be applied so that most of the remaining water is absorbed in the lens tissue, leaving behind about one optical fringe thickness. This remaining trace of water seems to evaporate, leaving a permanent bond between film and substrate.

Epitaxial liftoff (ELO) of the thin films takes place in dilute HF acid in a sealed beaker in a refrigerator at 0°C. After ELO, the acid is displaced by de-ionized (D.I.) water, and a foreign substrate is immersed in the beaker. The thin film, coated by wax (of trade name Apiezon W), is manipulated by a vacuum chuck and the initial bonding takes place without the ELO film ever leaving the aqueous environment into which it had been born. We find that D.I. water is a very clean environment for the initial bonding layers consist of 20-100 Å of native oxides. In the case of palladium coated substrates, however, the morphology is quite different as shown in Fig. 2, a TEM lattice image of an interface annealed at 200 °C for 30 min.

The ability of palladium to penetrate native oxides on semiconductor surfaces at low temperatures is a remarkable and technologically significant attribute. On GaAs, a deposited film of Pd diffuses through the typical native oxide layer at room temperature. The driving force for this diffusion, a solid-state topotaxial reaction forming the compound Pd$_x$GaAs ($x \approx 4$, hexagonal, isostructural with Pd$_3$Si), results in the mechanical dispersion of the native oxide layer allowing complete coverage of the interface with the reaction product. Kirkendall voids form in the unreacted Pd at the interface with Pd$_x$GaAs, a further indication that Pd is the dominant moving species.

The particular interface in Fig. 2 had been annealed at 200 °C, but the lattice image is very similar even when the annealing step is skipped. The native oxide appears to be displaced into Kirkendall voids which form ~200 Å below the GaAs/Pd$_x$GaAs interface, below the field of view in Fig. 2. For a sample simply allowed to stand at room temperature for 3 months, the Pd$_x$GaAs layer was found to be 60-Å thick. These observations are similar to those expected for a Pd film vapor deposited onto a GaAs sub-
an angular spread, indicating that the interfacial Pd$_4$GaAs crystallites are GaAs/Pd$_4$GaAs. The cubic GaAs spots are labeled with $h,k,l$ while the hexagonal Pd$_4$GaAs spots are labeled $h,k,l,il$. The Pd$_4$GaAs spots exhibit topotaxial alignment within about $5^\circ$ of the GaAs overlayer. The zone axes of the Pd$_4$GaAs and the GaAs are $[0 0 1]$ and $[1 1 0]$, respectively. The $[0 0 0 1]$ axis of Pd$_4$GaAs is in the plane of the image and parallel to the interface.

What is different here, of course, is that the GaAs substrate was a silicon wafer which had been coated with $500\,\text{Å}$ gold for adhesion, and then $600\,\text{Å}$ Pd. After ELO, the $p^+$-GaAs film, already partly metallized, was bonded to the Pd-created Si substrate by the Van der Waals bonding technique as described above. An anneal at $200^\circ$C completed the metallurgical bond to Pd$_4$GaAs. Then the individual metal contact pads on the $p^+$-GaAs film were isolated by wet GaAs etching, using the Au/AuZn/Cr metal contact pads themselves to define the GaAs dots, and the Pd layer as the etch stop between the dots. The final test structure was composed of $80\,\mu\text{m}$ (and larger) diameter $p^+$-GaAs dots contacted by standard ohmic metallurgy on top and by Pd$_4$GaAs below.

The experiment consisted of simply measuring the resistance between point contacts touching two different Au/AuZn/Cr metal pads. Current must flow through the two point contacts, two $p^+$-GaAs dots, two GaAs/Pd$_4$GaAs interfaces and then through the Pd film connecting the dots. We have measured a resistance of $(1.5 \pm 0.1)\,\Omega$, most of which can be attributed to contributions other than the GaAs/Pd$_4$GaAs contact. Therefore we can safely place an upper limit for the contact resistance $\leq 10^{-4}\,\Omega\,\text{cm}^2$. Similar results have been obtained on heavily doped $n^+$-GaAs ELO films.

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Mechanical tests of the adhesion of the GaAs ELO film on the Pd-created substrates were quite satisfactory after the $200^\circ$C anneal. A “Scotch” adhesive tape pull test showed that the entire film remained attached to the substrate, the only exception being when a dust particle prevented the solid-phase metallurgical reaction. More importantly, the Pd-bonded ELO film withstood a series of standard clean room processing steps such as photolithography, hard baking, rapid thermal annealing, spraying, etc. Likewise we may expect excellent thermal contact with the substrate through the Pd. Electrical contact to semiconductors, which generally involves the arcanet art of ohmic contact metallurgy, was well worth pursuing. Accordingly we proceeded to make the following test structure:

A $p^+$-GaAs film, doped $p \approx 2 \times 10^{19} \text{cm}^{-3}$, 1-μm thick, was grown on a 500-Å thick AlAs release layer, as is customary for ELO. Individual metallic contact dots, 250 nm thickness of Au/AuZn/Cr of varying diameters were deposited on the GaAs wafer by routine photolithographic techniques. This standard $p$-type ohmic metallization was alloyed in a rapid thermal annealer at $425^\circ$C. The target substrate was a silicon wafer which had been coated with $500\,\text{Å}$ gold for adhesion, and then $600\,\text{Å}$ Pd. After ELO, the $p^+$-GaAs film, already partly metallized, was bonded to the Pd-created Si substrate by the Van der Waals bonding technique as described above. An anneal at $200^\circ$C completed the metallurgical bond to Pd$_4$GaAs. Then the individual metal contact pads on the $p^+$-GaAs film were isolated by wet GaAs etching, using the Au/AuZn/Cr metal contact pads themselves to define the GaAs dots, and the Pd layer as the etch stop between the dots. The final test structure was composed of $80\,\mu\text{m}$ (and larger) diameter $p^+$-GaAs dots contacted by standard ohmic metallurgy on top and by Pd$_4$GaAs below.

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10. I. Pollentier and P. DeMeester (private communication).