A 720 mV open circuit voltage SiO_x:*c*-Si:SiO_x double heterostructure solar cell

E. Yablonovitch and T. Gmitter[a)]
Bell Communications Research, Murray Hill, New Jersey 07974

R. M. Swanson and Y. H. Kwark
Stanford University, Stanford, California 94305

(Received 29 July 1985; accepted for publication 10 September 1985)

For maximal performance solar cells should resemble semiconductor lasers, i.e., they should be constructed in the form of a double heterostructure. We have found rather good performance in SIPOS-crystalline silicon-SIPOS double heterostructure solar cells, where SIPOS≡SiO_x. The processing of these solar cells gives insights into the truly outstanding performance of the n^+-SIPOS:*p*-Si heterojunction which has a forward saturation current coefficient $J_0 = 10^{-14}$ A/cm^2, or equivalently an "emitter Gummel number" $G_e = 3.3\times10^{15}$ s/cm^4. This suggests that crystalline silicon solar cells can be much more efficient than had been suspected.

It has been recognized for some time that the structure of an ideal solar cell should resemble that of a semiconductor laser. The solar cell should be built in the form of a double heterostructure. In this configuration a narrow band-gap active layer is sandwiched between two wide band-gap layers of opposite doping. An example of a double heterostructure biased at a forward voltage V is shown in Fig. 1. The wide band-gap materials may be called "minority-carrier mirrors" although this term is more frequently applied to the high-low doping homojunctions at the rear of solar cells.

It is usually assumed that the wide band-gap heterocontact layers must be single crystal and lattice matched to the active layer to assure high performance. While this has been very successful for the III-V class of semiconductors, it is not actually a necessary condition. The wide band-gap layers need only be of sufficient electronic quality to support the quasi-Fermi level separation in the high quality narrow-gap active layer. Due to its larger band gap, the heterocontact material may be disordered and of poor quality and still be able to support the voltage generated in the active layer. That is the key point. The other main point is that the interface states at the heterocontacts must be passivated.

Since crystalline silicon has no useful lattice-matched heterocontacts, we turn to a disordered semiconductor heterojunction material, SIPOS (originally named semi-insulating polycrystalline silicon). In its annealed form it is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x). The interface states between SIPOS and crystalline silicon (*c*-Si) seem to be passivated as well as the high quality interface between thermally grown SiO_2 and *c*-Si.

The first indication of a superior quality heterojunction using SIPOS came in the pioneering[1] work at Sony. Matsushita *et al.*[1] showed that SIPOS heterojunction emitters incorporated as part of a bipolar transistor structure showed greatly enhanced current gains. A more direct measure of heterojunction quality is the forward saturation current J_0, where the forward current is given by $J = J_0 \exp(qV/kT)$, where J_0 should be as small as possible. An equivalent figure of merit[2] is the "emitter Gummel number" $G_e = qn_i^2/J_0$ which should be as large as possible. (Here q is the electronic charge and n_i is the intrinsic carrier density.)

As a result of the fabrication sequence to be discussed below we now routinely produce $J_0 = 10^{-14}$ A/cm^2 for n^+-SIPOS heterocontacts on *p*-Si (or equivalently $G_e = 3.3\times10^{15}$ s/cm^4). This is about two orders of magnitude superior to a conventional homojunction. Unfortunately we have been unable thus far to achieve a correspondingly good figure of merit for *p*-type SIPOS. Our best value of forward saturation current on *p*-type SIPOS is $J_0 = 8\times10^{-14}$ A/cm^2, which is nevertheless superior to that of a homojunction. Due to the lower quality of *p*-type SIPOS the solar cell we will describe falls short of the ideal of Fig. 1, in that both faces of the silicon wafer will be covered with n^+-SIPOS.

To achieve the highest possible open circuit voltage, electron-hole recombination in a solar cell must be minimized. There are two major recombination paths; on the surface of the active region and in the bulk of the active region. The purpose of a heterojunction contact is to minimize electron-hole recombination on the surface where electrical contact to one of the carriers is made. Equally important is the bulk recombination. This is minimized by using the highest quality silicon in as thin a crystal as permitted by optical absorption considerations. Recently, a quantitative analysis[3] of light trapping in semiconductor sheets showed that the effective internal path length for light rays in textured sheets was $4n^2 \approx 50$ times greater than the sheet thick-

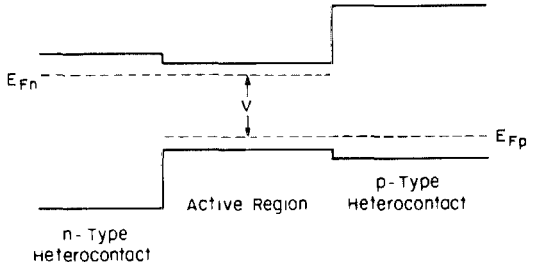

FIG. 1. Ideal solar cell would be in the form of a double heterostructure, by analogy with semiconductor lasers. $V = E_{Fn} - F_{Fp}$ represents the quasi-Fermi level separation.

[a)] Part of this work was performed while the first two authors were with Exxon Research & Eng'g. Co., Annandale, NJ 08801.

 0003-6951/85/231211-03$01.00

TABLE I. Properties of silicon wafer material.

Orientation	⟨100⟩
Resistivity	0.5 Ω cm p-type
Doping concentration	2.5×10^{16}/cm^3
Bulk minority-carrier lifetime	450 μs
Minority-carrier mobility	700 cm^2/Vs
Diffusion length	0.9 mm
Thickness	50 μm
J_0 of n^+-SIPOS heterocontact	10^{-14} A/cm^2 at 27 °C
Emitter Gummel number	3.3×10^{15} s/cm^4

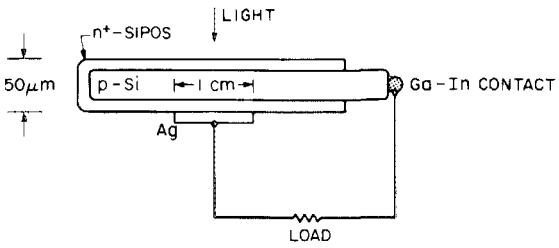

FIG. 2. Test configuration for the SIPOS : c-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the p-Si wafer itself.

ness (where n is the index of refraction). Accordingly, the optimum[4] thickness of silicon solar cells is $\approx 50\,\mu$m, much thinner than would be the case without light trapping.

In this work we used float zone p-type silicon wafers of 0.5 Ω cm resistivity which were chemically thinned to 50 μm. The material properties are summarized in Table I, and the sequence of processing steps for the SIPOS deposition in Table II. Step (2) in Table II is critical in achieving a bulk minority-carrier lifetime of 450 μs. The as-received material is only about half as good.

The silicon wafers, which were coated on both faces with 1000 Å of n^+-SIPOS, were fabricated into devices as shown in Fig. 2. The n^+-SIPOS was contacted with a 0.5 cm × 1 cm evaporated silver electrode. The p-Si was contacted by Ga-In metal at one edge of the wafer. No attempt was made to optimize the current collection or the fill factor in this design. The series resistance was dominated by the bulk resistance of the wafer itself between the edge contact and the active region. This limited the fill factor to about 0.5.

The open circuit voltage was measured under a simulator at 1.3 suns. The light intensity was calibrated by two separate standard solar cells obtained from SERI. An intensity slightly above one sun was chosen in order to partially compensate for the absence of an antireflection coating on the silicon wafer and to simulate one sun absorbed internally. The measured open circuit voltage[5] was 720 mV at 25 °C, with relatively small variations from run to run.

This outstanding voltage performance is made possible both by the excellent bulk quality of the crystalline silicon and the excellent surface passivation of the n^+-SIPOS heterocontact. The bulk leakage current is 1.5×10^{-14} A/cm^2 for the bulk parameters in Table I while the surface component of 10^{-14} A/cm^2 must be multiplied by 2 for the two faces of the wafer. This gives an overall $J_0^{\rm tot} = 3.5\times10^{-14}$ A/cm^2, which is responsible for the observed open circuit voltage.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

The forward saturation current J_0 of the SIPOS heterocontact was checked in two ways in addition to the implicit check associated with the measured open circuit voltage. One method was to fabricate bipolar transistors using SIPOS emitters[6] and to measure the transistor characteristics. Another method was to measure the photoconductivity decay lifetime[7] on wafers with known[8] excellent bulk lifetime and known bulk doping density. Especially for thin wafers, surface recombination will dominate and the resulting data can be used to determine J_0. The connection is expressed by $J_0 = qn_i^2 S/p^b$, where S is the observed surface recombinatin velocity and p^b is the bulk majority-carrier density. All these diagnostic methods agree and give $J_0 = 10^{-14}$ A/cm^2 for wafers subjected to the processing sequence in Table II.

Of critical importance in achieving this performance level is the oxidation step (6). In omitting that one step the "emitter Gummel number" figure of merit degrades by almost an order of magnitude. We found that purging with high-purity cylinder gas (<0.5 ppm O_2 and H_2O) helps to reproducibly control this oxidation step. In some published[1,9,10] results on SIPOS heterojunction emitters and polysilicon emitters this step has been omitted, but we believe that oxidation frequently occurs inadvertently and is necessary toward achieving the most favorable figure of merit. Dewar nitrogen gas is notoriously unreliable in regard to oxygen concentration and was avoided. Likewise it was helpful to load the silicon into a cold furnace to prevent inadvertent oxidation.

The annealing step (9) follows SIPOS deposition. This step is necessary to precipitate microcrystalline silicon grains within the material and to activate the phosphorus dopant. In addition during this step the phosphorus diffuses about 20–50 Å into the silicon wafer as measured by secondary ion mass spectrometry. This produces a very shallow n^+ accumulation layer which is transparent to minority carriers; i.e., the holes from the bulk "see" the Si-SiO_2 interface. Recent studies[11] of electron-hole recombination at thermally grown Si-SiO_2 interfaces have shown that under accumulation the recombination current is $\exp(qV/kT)\times10^{-14}$ A/cm^2, which is consistent with the performance level achieved with the SIPOS emitter structure in Fig. 3.

Oxide thickness between 25 and 40 Å was found to be equally favorable with respect to the "emitter Gummel number." Therefore, differential tunneling between electrons and holes does not appear to be playing a major role because

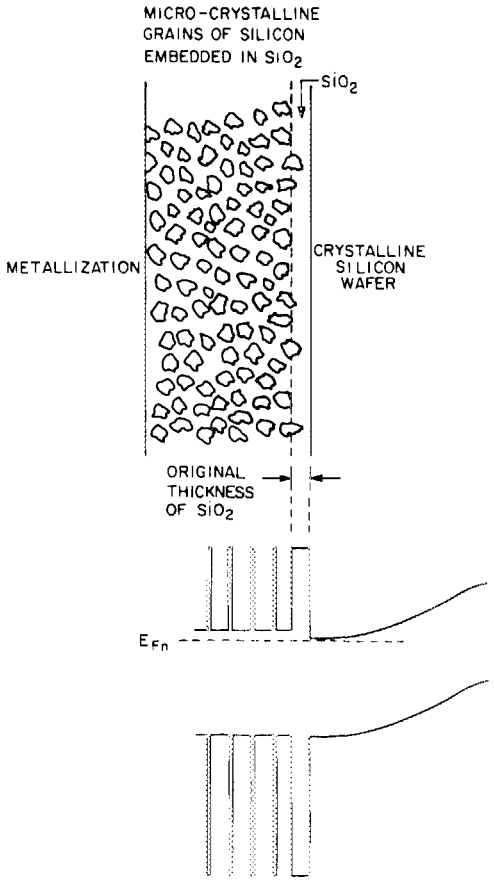

FIG. 3. Model for the metallurgical configuration of the SIPOS-Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

over part of this range the oxide is too thick for electron tunneling. We believe the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO_2. The chemical mixture in step (7) of Table II results in a SIPOS formulation with only 5% oxygen incorporation as determined by x-ray fluorescence. At such low levels of oxygen concentration one might ask what distinguishes a SIPOS heterojunction from a polysilicon emitter. Indeed the resistivity of the n^+-SIPOS ($\rho = 10^{-3}\ \Omega$ cm) is similar to that of doped polysilicon. We believe the importance of the 5% oxygen concentration is metallurgical rather than electrical. The small concentration of oxygen inhibits grain growth and causes a microcrystalline structure with a significant surface density of individual grains protruding into the thin oxide layer. In polysilicon the grains are much larger, reducing the density of potential contacting points and causing reproducibility and repeatability problems.

We see then that the functioning of the n^+-SIPOS heterojunction shown in Fig. 3 is complex. The individual contacts provide more than enough conductivity for majority-carrier electrons, but the small fractional contact area acts to block minority-carrier holes from recombining in the SIPOS. Differential tunneling probability between electrons and holes is probably not playing a major role, since such a process would be very sensitive to oxide thickness contrary to what we observe. The functional mechanism of the n^+-SIPOS: p-Si heterojunction emitter will be discussed at greater length in a forthcoming[12] publication.

The results in this letter suggest that a nonconcentrator crystalline silicon solar cell can be designed to achieve an efficiency of 24% under air mass 1 illumination. This design would rely on superior heterojunction emitters to improve the voltage and on light trapping[3] to improve the current in a thin device. The recent achievement[13] of 25% efficiency in a c-Si concentrator cell (without the benefit of light trapping) should be regarded as further encouragement along these lines.

[1]T. Matsushita, N. Oh-uchi, H. Hayashi, and H. Yamoto, Appl. Phys. Lett. **35**, 549 (1979).
[2]H. C. DeGraaf, J. W. Slotboom, and A. Schmitz, Solid State Electron. **20**, 515 (1977).
[3]E. Yablonovitch and G. Cody, IEEE Trans. Electron Devices **ED-29**, 300 (1982); E. Yablonovitch J. Opt. Soc. Am. **72**, 899 (1982).
[4]T. Tiedje, E. Yablonovitch, G. D. Cody, and B. G. Brooks, IEEE Trans. Electron. Devices **ED-31**, 711 (1984).
[5]E. Yablonovitch, R. M. Swanson, and Y. H. Kwark, *The Conference Record of the Seventeenth IEEE Photovoltaic Specialists Conference—1984* (IEEE, New York, 1984), p. 1146.
[6]Y. H. Kwark, "SIPOS Heterojunction Contacts to Silicon," Technical Report, Solid State Electronics Laboratory, Stanford University, 1985.
[7]G. L. Miller, D. A. H. Robinson, and S. D. Ferris, Proc. Electrochem. Soc. **78-3**, 1 (1978)
[8]Chemical methods (fluorination) were to be used to minimize surface recombination and permit a measurement of the bulk minority-carrier lifetime. B. R. Weinberger, H. W. Deckman, E. Yablonovitch, T. Gmitter, W. Kobasz, and S. Garoff, J. Vac. Sci. Technol. A **3**, 887 (1985).
[9]M. B. Rowlandson and N. G. Tarr, IEEE Electron Device Lett. **EDL-6**, 288 (1985).
[10]B. Soerowirdjo and P. Ashburn, Solid State Electron. **26**, 495 (1983).
[11]E. Yablonovitch, R. M. Swanson, W. E. Eades, and B. R. Weinberger, Appl. Phys. Lett. (to be published).
[12]E. Yablonovitch and T. Gmitter, Electron Device Lett. Nov. (1985).
[13]R. Sinton, Y. H. Kwark, S. Swirhun, and R. M. Swanson, IEEE Electron Device Lett. **EDL-6**, 405 (1985).