Fundamental Conductance ÷ Voltage Limit in Low Voltage Tunnel Switches

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***Abstract*— There is a fundamental conductance ÷ voltage limit in low voltage (<4k$_b$T/q) tunneling switches that turn off by relying upon the band edges to cutoff the available density of states. The Fermi occupation probabilities are thermally broadened by 4k$_b$T. However, current is only allowed to flow in a narrow energy range limited by the applied voltage, V. This means that if a voltage less than 4k$_b$T/q is applied, the conductance will be reduced by at least qV/4k$_b$T. Even with a perfect tunneling probability of 1 in a perfect quantum channel, the conductance quantum would be diminished by qV/4k$_b$T. Attempts at lowering the operating voltage below <4k$_b$T/q must come at the expense of smaller conductance.**

***Index Terms*— Tunneling field effect transistor (TFET), density of states, tunneling, energy filtering, thermal broadening.**

I. Introduction

TUNNELING Field Effect Transistors promise to dramatically reduce the voltage and thus power consumption of modern electronics by overcoming the thermally limited subthreshold swing voltage of 60mV/decade [1], [2]. The sharpest turn-ons can be achieved by using the bandedge energy filtering or density of states overlap mechanism [3]. If the conduction and valence band don't overlap, no current can flow. Once they do overlap, there is a path for current to flow. However, as we will show in the next section, when the supply voltage, V_{dd}, is less than 100 mV at room temperature ($4k_bT/q$) there is a fundamental tradeoff between voltage and conductance.

II. Fundamental Tradeoff Between Voltage and Conductance

To understand what happens in a tunneling junction at low voltage, consider the simple pn-junction in Fig. 1(a). Tunneling is occurring from the partially filled valence band on the pside to the partially empty conduction band on the nside. The overlap between the conduction and valence bands is defined as $E_{OL} = qV_{OL}$ as shown in Fig. 1(a). The voltage, V_{SD}, is applied between the contacts. This determines the Fermi level splitting: $qV_{SD} \equiv E_{FC} - E_{FV}$. The overlap voltage, V_{OL} is controlled by V_{SD} and by V_G, the gate voltage, in a transistor.

Manuscript received August 1, 2014; accepted August 16, 2014. Date of publication September 11, 2014; date of current version September 23, 2014. This work was supported by the Center for Energy Efficient Electronics Science, National Science Foundation, under Award 0939514. The review of this letter was arranged by Editor S. J. Koester.

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Digital Object Identifier 10.1109/LED.2014.2350434

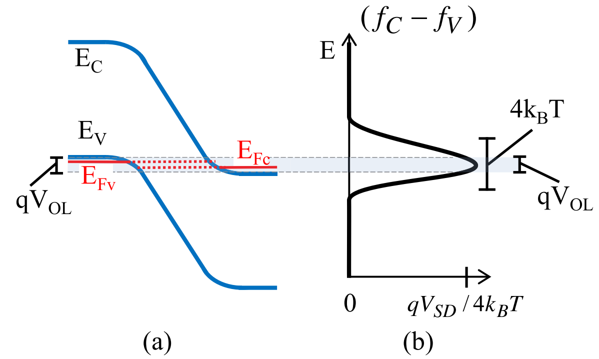

Fig. 1. (a) Electrons can only tunnel in a narrow energy range given by V_{OL}. (b) The thermal occupation difference is spread out over a $4k_bT$ energy range. Consequently, the conductance will be reduced by a factor of $qV_{OL}/4k_bT$.

Electrons can only tunnel in a narrow energy range given by V_{OL}. However, the thermal occupation difference is spread out over a $4k_bT$ energy range. This means that the conductance will be reduced by a factor of $qV_{OL}/4k_bT$ when V_{OL} and V_{SD} are less than $4k_bT$.

Algebraically, we can see this by Taylor expanding the Fermi functions ($f_c - f_v$) in the 1d tunneling current [4]–[6]:

$$I = \frac{2q}{h}\int_0^{qV_{OL}} (f_C - f_V) \times \top \times \partial E \tag{1}$$

The tunneling probability is given by $\top$ and often given by a simple WKB approximation. In the small bias regime:

$$f_c - f_v \approx \frac{(E_{Fc} - E_{Fv})}{4k_bT} \approx \frac{qV_{SD}}{4k_bT} \tag{2}$$

Plugging this back into (1) gives:

$$\begin{aligned} I &\approx \frac{2q}{h} \times \frac{qV_{SD}}{4k_bT} \times \int_0^{qV_{OL}} \top \times \partial E \\ &= \frac{2q^2}{h} \times \langle \top \rangle \times V_{SD} \times \frac{qV_{OL}}{4k_bT} \end{aligned} \tag{3}$$

where $\langle \top \rangle$ is the energy averaged tunneling probability. The conductance is given by:

$$G = I/V_{SD} = \frac{2q^2}{h} \times \langle \top \rangle \times \frac{qV_{OL}}{4k_bT} \tag{4}$$

If the tunnel junction is in 2 or 3 dimensions, Eq. (4) needs to be multiplied by the number of transverse modes, $N_{\perp\text{modes}}$ [4], [5]. The overlap voltage must be less than the overall supply voltage, $V_{OL} < V_{dd}$, in order to allow the

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switch to turn off. The tunneling probability is also less than 1. Consequently, we arrive at the following inequality:

$$G < \frac{2q^2}{h} \times N_{\perp \text{modes}} \times \langle \top \rangle \times \frac{qV_{DD}}{4k_bT} < \frac{2q^2}{h} \times N_{\perp \text{modes}} \times \frac{qV_{DD}}{4k_bT} \quad (5)$$

This results in a fundamental conductance/voltage ratio inequality:

$$\frac{G}{V_{dd}} < \frac{q^3}{2hk_bT} \times N_{\perp \text{modes}} \quad (6)$$

The inequality says that low voltage switches inherently have poor conductance in the on-state, while high-conductance switches require $V_{dd} > 4k_bT$(in addition to a high tunneling probability). The lower conductance directly reduces the speed through the RC time or the gm/C frequency.

At small biases less than $4k_bT$, the thermal broadening of Fermi occupation probabilities will have the same impact on the off state as in the on-state. Consequently, the thermal broadening will not have any effect on the on/off ratio.

We can quantitatively understand the inequality by considering a 2d quantum well. The energy averaged number of transverse modes, $N_{\perp,\text{QW}}$ is given by [4] and [5]:

$$N_{\perp,\text{QW}} = \frac{2}{3}\left(\frac{L\sqrt{m^*}}{\pi\hbar} \times \sqrt{qV_{OL}}\right) \quad (7)$$

Plugging in an effective mass of 0.1 and using the fact that $V_{OL} < V_{dd}$ gives the following inequality:

$$G < 5.8\frac{mS}{\mu m} \times \langle \top \rangle \times \left(\frac{V_{DD}}{100mV}\right)^{3/2} \quad (8)$$

An ideal tunneling junction with $\top = 1$ that switched in 10mV would have a maximum conductance of 183 μS/μm and current of 1.8 μA/μm.

III. Conclusion

There is a fundamental conductance÷voltage limit in energy filtering TFETs due to thermal broadening. As the operating voltages are reduced below 100 mV ($4k_bT$ at room temperature), the transistor conductance will be reduced by at least $qV_{DD}/4k_bT$. Consequently, when operating at 10 mV, the conductance and thus transistor speed will be reduced by a factor 10. Even if a perfect tunneling probability of 1 could be achieved, a perfect quantum of conductance at voltages less than $4k_bT$ cannot be achieved!

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