

Transistor-Based Ge/SOI Photodetector for Integrated Silicon Photonics

By

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Abstract

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This dissertation describes our effort on developing a technology of photodetectors for application in chip-level optical communication. The photodetector proposed in this thesis work is the Ge/SOI Photo-Hetero-JFET. It is based on a silicon junction-FET in which the traditional electrical gate is replaced by a photo-active germanium mesa. The silicon channel conductance is then modulated by near-infrared light signal incident on the germanium gate.

The limitations of traditional electrical wires which restrict the performance of microelectronic information systems drive researchers to look at optical interconnects as a good alternative for inter-chip data communication. One of the major challenges that the optics solution faces is to achieve as low energy consumption as 100aJ/bit. This in turn sets stringent requirements on the sensitivity of photodetectors, which can only be achieved when the photodetector can be highly integrated and has extremely small device capacitance ($<1\text{fF}$). The Ge/SOI Photo-Hetero-JFET is seamlessly integratable with microelectronic circuitry and also scalable to achieve extremely small capacitance. It was therefore proposed as a promising photodetector design for the application to inter-chip-scale optical links.

Ge/SOI Photo-Hetero-JFETs with gate length of 100nm are fabricated. They were then characterized as near-infrared photodetectors both under continuous-wave laser and pulsed laser at 1550nm. Geminate recombination together with severe SRH recombination of photocarriers in the germanium gate is found to significantly limit the responsivity of the photodetector. Nonetheless, after correcting for the poor internal quantum efficiency, we found that *one collected photons can lead to the generation of ~ 750 electrons in the silicon channel*, which indicates a DC secondary photoconductive gain of 750 on top of primary responsivity.

Time-resolved measurement done on the Photo-Hetero-JFET further reveals that the photodetector can respond to laser pulses as short as 4ps. Although the observed risetime of transient photoresponse is 50ps which is currently limited by bandwidth of the measurement circuit, it is believed that when the photodetector is fully-integrated it can achieve its inherent risetime of ~ 1 ps! One caveat regarding the Photo-Hetero-JFET is that its transient photoresponse has a long tail (~ 26 ns fall-time). This was originally attributed to dielectric relaxation process of trapped holes in the gate, but is later found to result from the dispersive nature of photocarrier transport in the defective germanium mesa. In the analysis of peak transient amplitude through JFET model based on trapped charges, we found that with the design of Photo-Hetero-JFET *only ~ 50 photo-holes on the gate/channel junction of $0.1\mu\text{m}^2$ can induce channel current of $\sim 5\mu\text{A}$!* This proves that Photo-Hetero-JFETs can also achieve high sensitivity under pulsed illumination.

The attributes of the Photo-Hetero-JFET design that makes the device highly sensitive is its extraordinarily small device capacitance (~ 52 aF) and its seamless integrability with silicon circuitry. Currently, the fabricated Photo-Hetero-JFETs suffer from poor quantum efficiency and slow gain which were brought about by the poor germanium quality. Nonetheless, the device still presents impressive secondary photoresponsivity and great potential in its bandwidth improvement. It is believed that with reasonable germanium film quality, (diffusion length of ~ 100 nm already available in the industry), the Photo-Hetero-JFET is capable of demonstrating great sensitivity and fast speed in the application of chip-level optical communications.

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Dedicated to
My parents for their love and guidance

Chapter 1 Introduction

This dissertation describes our effort in creating a technology of photodetectors which can accelerate the realization of chip-level optical interconnects. The criteria that are being sought, in such photodetectors in alignment with those of optical interconnect technology, are high integration with silicon circuitry and great photo-sensitivity.

This introductory chapter begins with a brief description of the background and discussion of the motivations of our work. The reasons why optical interconnects are a most promising candidate to replace problematic electrical wiring at the chip-level are summarized. The challenges that chip-level optical links are facing are presented, and the conclusion they lead to, in terms of the receiving end, is that, very sensitive germanium photodetectors with extremely small device capacitance are essential. Then different forms of phototransistors are discussed and reviewed. Finally, the organization of the dissertation is presented.

1.1 Motivation

As the microelectronic systems continue to scale down along the projection by Moore's Law, the individual logic elements in the systems have become significantly smaller and faster. Computational speed of the systems is therefore no longer limited by the individual logic elements, but by the communication between them. Indeed, this bottleneck is considered as one of the biggest challenges in the future advancement of integrated electronics [1].

Traditional electrical wiring historically has been an efficient and economic means of communication at various levels of electronic systems, and currently it still dominates the links in and between electronic chips and circuit boards. However, as the volume of chip-to-chip and on-chip communication rockets up, due to the inherent physical properties of electrical wires, it becomes increasingly difficult for them to cope with the growing bandwidth demand. For this reason, optical links have been proposed as a most promising candidate to replace electrical wires and revolutionize the chip-level communications. As a matter of fact, optical fibers have long taken over electrical cables in long-haul telecommunication and optical data links are now extensively employed between cabinets in large systems too. Nonetheless, to use optics at ever shorter distances, all the way down to inter- and even intra- electronic chips, there are technological challenges to solve.

1.1.1 Limitations of electrical wires

One of the limitations of electrical wires is that they are inherently lossy [2]. Resistance

of the conductors, together with other factors including dielectric loss, causes electric signal to attenuate. Such attenuation is usually worse for higher frequencies, which leads to distortion of signals. There are techniques such as amplification and equalization that can be used to compensate attenuation and distortion to some extent, and advanced signal formats and signal processing are also used to maximize the information capacity in presence of these imperfections [3]. However, all these techniques increase the complexity of the system and hence increase cost and power dissipation.

It seems that a simple solution to increase information capacity for a given wire is to increase its cross-sectional size, which reduces its resistance. But this increases costs for long lines and also limits the density of wiring in large complex systems. In fact, in these systems, the limited available space tends to be filled with wiring, and equally importantly, to be used to deliver power and remove heat from the system. In this sense, information processing systems tend to be simultaneously limited by wiring density and power [3].

It is found that one cannot increase the information capacity either, by simply scaling down the wires and increasing the wiring density. For bulk-resistance-limited RC lines, scaling down a wire in all three dimensions leaves the RC product the same (Fig.1-1), and if the RC product characterizes the minimum allowable bit time for simple on-off signaling, then such scaling has no effect in changing the number of bits per second that can be transmitted through the wire. For skin-effect-resistance-limited LC lines, the scaling of information capacity for simple on-off signaling follows a similar scaling law. It is actually shown that, at least with a simple model of on-off signaling, the capacity of electrical lines from such resistive limits obeys approximately [2]

$$B \leq B_o \frac{A}{L^2}, \quad (1.1)$$

where A is the cross-sectional area of the wiring, L is the length of the wires, and B_o is a constant (~10¹⁶ bits/s for RC-limited lines and a slightly smaller number for LC-limited lines). Equation (1.1) also holds if A is the total cross-sectional area of the wires, not just of one wire. Therefore, by packing smaller wires more densely into a system won't help in increasing the information capacity. It doesn't help either by making the system smaller or bigger once all available space is filled with wiring.

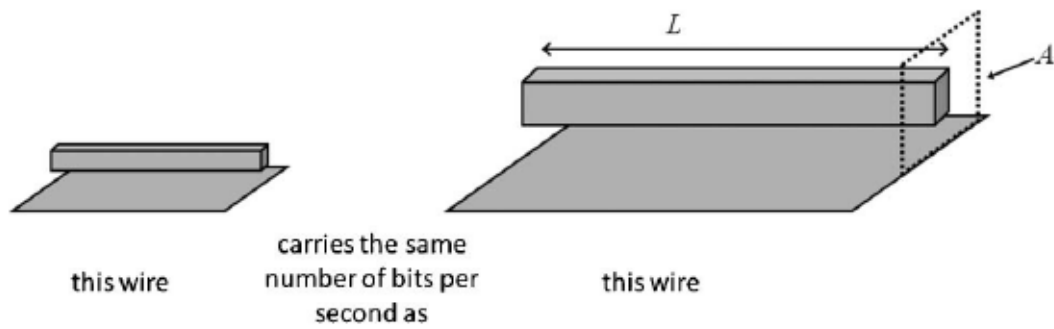


Fig.1-1 Simple scaling of electrical wiring does not change the RC product. For simple signaling where the RC product would set the shortest pulse to be readily sent on the line, the bit rate capacity of the line is unaffected by the simple scaling (reproduced from ref. [2]).

Going beyond simple scaling, there are signal compensation and sophisticated signal processing techniques to expand the information capacity. But as we mentioned previously, these surely raise the costs as one tries to push past the scaling limitation to the information density in electrical wires. The physics of electrical lines also leads to other problems in signal integrity for dense and high speed wiring, including slow effective signal propagation velocities (e.g., ~5% of the velocity of light), and cross-talk between adjacent wires. The limited bandwidth of electrical wiring also limits the time precision for clock distribution.

Apart from wiring density, interconnect energy also limits the performance of modern information processing systems. In fact, among three core operations - logic switching, memory and interconnect, it is the interconnect that accounts for most of the energy dissipation [3], and that energy is almost all associated with charging and discharging the capacitance of electrical wires. For example, in a CMOS gate [4], the capacitance of the transistor is roughly equal to the capacitance of a wire connecting this gate to the adjacent one. So the energy associated with charging or discharging transistor capacitance should be on the same scale of charging or discharging that short interconnect line. For information sent further than the adjacent gate, the energy for charging or discharging the interconnect line can easily exceed that required for the switching of a logic gate. In memory banks, however, the energy dissipation on the interconnect lines is even more severe since memories are usually addressed while whole sets of lines are charged or discharged in reading or writing a single cell. So again the reading and writing energy - energy dissipated in interconnect lines - is much larger than that required to retain a bit of information reliably in the memory cell. Other sources of energy dissipations in information processing systems include static dissipations associated with leakage and subthreshold currents. Also, for each unit of energy spent on the core operations, approximately equal or greater energy is to be spent on supplying and conditioning power and sinking thermal dissipation. In fact, information processing systems are increasingly

constrained by energy dissipation. Since interconnect energy dominates energy dissipation of the core operations, and can possibly dominate that of the entire signal processing, it is imperative to find ways to reduce the energy dissipated in the interconnect lines.

In short, with electrical interconnects, wiring density and energy are two main issues that hamper the advancement of signal processing systems. The inherent properties of electrical wires, however, determine that one can only minimize these problems to some extent with sophisticated schemes at the expense of system costs. Therefore, a fundamentally different interconnect technique needs to be available to completely solve the existing problems.

1.1.2 Advantages of optical interconnects

Optical interconnects have been proposed as one of the promising candidates to replace traditional electrical wires. In long-haul telecommunication systems, optics has long been the sure choice of communication thanks to extremely low loss and low dispersion of optical fibers. The technical optimization at that system scale is basically designing the fiber system to operate over the longest possible distance with highest possible bandwidth, and thereby the size, power dissipation and even cost of optical transmitters and receivers are of secondary importance. However, when it comes to interconnects at shorter distances, interconnect density and power dissipation are of particular importance [3], neither of which is critical at longer distances.

The use of optics can improve the density of interconnections in the systems with shorter interconnects. The reason behind it is that optical fibers or waveguides do not have the resistive loss physics that limits the capacity of electrical wires [2]. This density advantage is one major reason that has been driving the introduction of optics between cabinets, inside machines and onto chips. For interconnections between backplanes, although electrical cables can carry substantial amount of information over that distance, optical cables however can perform the same job with much smaller cable diameters, and as a result, with greater connection densities. For ever shorter interconnections, especially at chip-level, optical links with the density benefit offer us with a prospect to overcome the notorious scale-invariance of the capacity of electrical wires. In addition, the use of wavelength-division-multiplexing (WDM) further boosts the information capacity of optical channels. In fact, optical fibers themselves are capable of carrying extraordinarily high densities of information. For example, single-mode telecommunication fibers, with a diameter of only 125 μm , can carry tens of terabits per second of information [5]. Admittedly, preparing the information in the right form to exploit that bandwidth is never a simple task, and involves many high-speed transmitters and receivers as well as sophisticated wavelength-division multiplexing. Nonetheless, with fiber itself or optical

waveguide there is practically no limit to the information capacity for the foreseeable future [3].

Severe power dissipation of electrical wiring is another major constraint on the performance of information processing systems. For optical interconnects or any other technologies to replace copper wires, they must consume much less power than their electrical counterpart. One might argue that this does not seem to be an advantage for optics at all, since in the long distance optical communication, transmitters and receivers typically consume significant amounts of power, and thus one would not expect that the same technology employed at shorter distance would offer advantage in power dissipation. The reason behind this opinion at first glance is that the main strategy in designing the long distance optical communication is to work with the minimum received optical power, not the *minimum total energy per bit communicated*. But when it comes to interconnects at short distances, the total energy per bit, including the power of both the transmitter and receiver, becomes the primary concern [3].

The remarkable quantum-mechanical nature of optics readily offers the benefit of power efficiency, making optical interconnects fundamentally different from electrical wires. While in electrical systems, the energy required is at least that needed to charge the line (or at least the section of the line that corresponds to the length of the electrical pulse) to the signal voltage. In optical systems, the signal voltage that is generated in a photocell is weakly connected to the power for the light beam. In other words, the voltage can remain constant - numerically equal to the photon energy in electron volts, even if the optical power is tuned down. This eliminates the need to “charge” the optical line fully to the signal voltage. Another aspect of looking at this is “quantum impedance conversion” [6], i.e. the quantum detection in the optical case effectively matches the high impedance of small devices to the low impedance of the electromagnetic propagation ($\sim 50\Omega$ in cables, $\sim 377\Omega$ in free-space propagation).

It has been realized that in optical interconnects at shorter scale, the primary goal of minimizing energy per bit communicated is not the same as optimizing for the minimum received energy, since the energy required to run the receiver amplifier to boost up that minimum signal may well exceed the energy “saved” earlier. For the exact same physics that cell phone batteries go away very fast in weak signal zone, the receiver amplifiers tend to consume much more power if it is operated under weak signals, in fighting with the thermal noise limit. Hence, it is not surprising that in minimizing the total energy dissipated per bit in a short link, the strategy that finally comes out is to deliberately use more received photons to prevent the receiver amplification stages from being noise-limited [7], and requiring more receiver power.

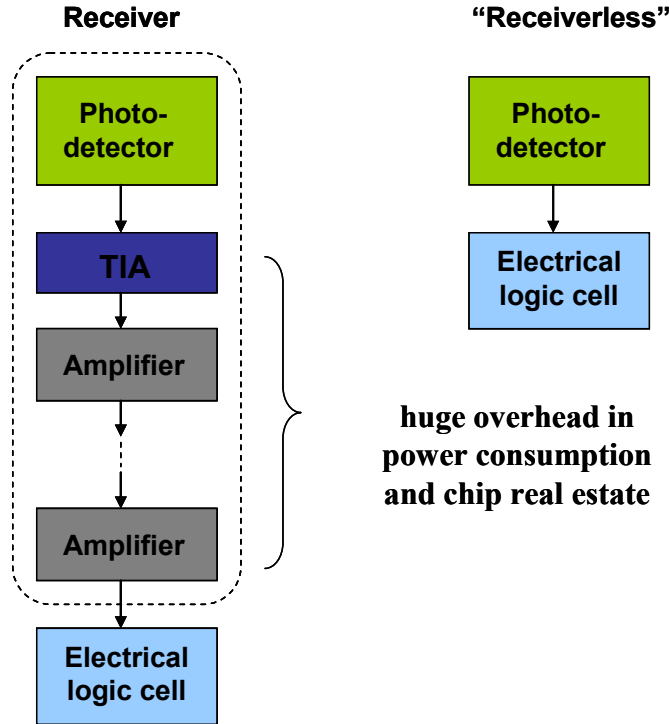


Fig.1-2 Traditional receiver configuration in comparison with “receiverless” configuration

It is even desirable to run the receiving end of an optical link without amplification stages. In a traditional optical receiver, the photodetector converts an optical signal into electrical current which is later converted to electrical voltage by a trans-impedance amplifier. The voltage is then amplified by subsequent amplification stages before it is sent to the logic unit (see Fig.1-2). Obviously, this configuration has huge overhead in power consumption and chip real estate. So in face of energy and density constraints on the interconnect technologies, there’s indeed an urge to get rid of all the amplifications in the receiver and operate the photodetector “receiverless” [8]. It is also entirely possible to have input optical pulse with sufficient energy to swing the photodetector over a full logic range. The key point is that interconnect receivers should have extremely low photodetector capacitance. For instance [3], with total detector and input transistor capacitance of 1fF, a fJ of 1eV photons (~6000 photons) would generate ~1V swing in the photodetector. It should be noted that 1fF of detector capacitance is readily achievable in micrometer-sized detectors integrated beside or within the receiver transistors. The energy benefit of optics from quantum impedance conversion applies to the transmitter side as well, but since this thesis work is devoted to the receiving end of the chip-level optical links, we would not dwell on the discussion of transmitter here.

In addition to density and energy benefits, optics offers improved signal integrity and timing [3]. Low dispersion of optical channels permits the propagation of short pulses

over long distances without being substantially broadened, and thereby ensures the precise timing of signals. Another reason for improved timing precision is that the propagation velocity of optical signals is less temperature dependent than that of electrical ones. Optical interconnects should have reduced cross-talk too, and even if there is cross-talk, it is not dependent on bit rate which is always much lower than the carrier frequency.

With all the benefits that optics enjoys, optical interconnect boasts great potential to replace electrical wiring. However, as the technology of electrical interconnects has evolved to be very advanced and inexpensive, for optics to have more compelling reasons to replace its electrical counterparts, certain technological challenges have to be met.

1.1.3 Challenges for optical interconnects

The technology of optical interconnects at short distances, especially down to chip-levels, is still immature in competition with that of electrical wiring. That's why in spite of all the problems and constraints mentioned above, wires still convey the traffic within and between chips. Admittedly, the technologies associated with long distance optical communication are quite developed, but they cannot be readily transferred to the technology of dense, short-distance optical interconnects, as they were not designed for the same optimization criteria. While optical data links are currently being used extensively between backplanes and boards, at even shorter scale, i.e. chip-level communications, they haven't proven an obvious advantage in power efficiency over electrical wires

The energy dissipation for electrical wiring at different length scales is estimated as follows. The total dissipations of present high-performance electrical interconnects on backplanes are in the scales of a few tens of pJs per bit. For connections on and off chips, energies of several pJs per bit can characterize up-to-date low-energy interconnects. When it comes to the global interconnect lines on chips, $\sim 1\text{pJ/bit}$ is a typical number [9]. Based on these state-of-the-art numbers for electrical wiring, when we seek solutions with optics, we should aim at targeted energies at least one order of magnitude lower, which means $\sim 1\text{pJ/bit}$ for backplane connections, and $\sim 100\text{fJ/bit}$ for intra-chip and global on-chip wiring. The reason to set the target an order of magnitude lower is to leave enough margins to justify serious consideration of replacing electrical wires with optical interconnects.

Now that the total system energy is set to be 100fJ/bit , the estimated received optical energy would be $\sim 1\text{fJ/bit}$ [3]. Note that this estimated value is obtained after taking into considerations of various losses and energies dissipated in performing driver, receiver and etc. As analyzed earlier, to generate substantial voltage ($\sim 1\text{V}$) with 1fJ photons of

$\sim 1\text{eV}$ to drive the logic gate, the total photodetector-plus-transistor capacitance should be as low as 1fF . This extremely small capacitance is only possible for photodetectors fully integrated with the circuitry on chip, since a wire of only $10\mu\text{m}$ length already has capacitance of a few pFs. Therefore the technological challenge for chip-level optical interconnects at the receiving end is to have a photodetector which is *highly-integrated* and has *extremely small device capacitance*. This is exactly how we were led to our design of Ge-on-SOI Photo-Hetero-JFETs.

Similarly, there are technical challenges for optical output devices like lasers and modulators at the transmitter end of the optical link. The energies of these optical output devices need to be in the scale of a few tens of fJ/bit and these devices need to be well-integrated to minimize its capacitance too [3]. Vertical cavity surface emitting lasers are likely to be 1pJ/bit systems, and 100fJ/bit systems would require more radical lasers like nanocavity lasers [9]. But those lasers cannot be easily integrated with silicon. Modulators with an external light source is a feasible strategy. Admittedly, silicon-based modulators suffer from the weak electro-optic effect in Si, and the use of high Q resonators requires precise temperature control. Nonetheless, high-Q resonator Si modulator and other CMOS compatible modulators, such as germanium modulators based on Franz-Keldysh effect [10] and germanium quantum wells based on quantum-confined Stark effect (QCSE) [11,12], can still be good candidates for on-chip optical output devices. Since this thesis work is devoted to photodetectors in the application of chip-level optical communications, we will leave the discussion of the transmitter end, and in the following section, we'll review various germanium photodetectors reported from literature.

1.2 Review on Ge photodetectors

Major advances made in recent years in the field of silicon photonics have a path well aligned with research in chip-level, short distance optical communications. Germanium-based photodetectors are certainly one of them. The reason for choosing germanium over other semiconductors as a photodetector material is that it can be grown in CMOS compatible processes for ease of integration with silicon and it absorbs well at communication wavelengths ($1.3\mu\text{m}$ and $1.55\mu\text{m}$) where attenuation and dispersion in fibers are lowest (Fig.1-3). Other reasons in choosing germanium photodetectors over silicon include higher carrier mobility in Ge which promises faster operation.

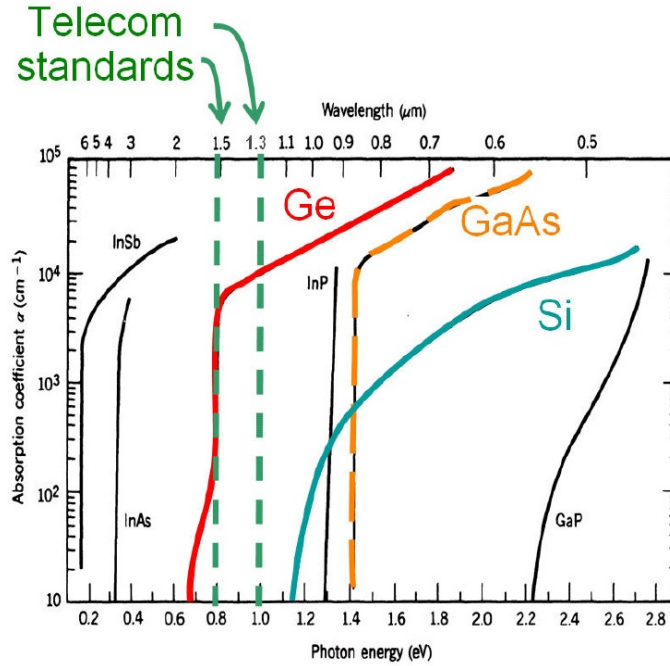


Fig.1-3 Absorption coefficient for various semiconductor vs. photon energy (reproduced from ref. [1])

Different types of germanium photodetectors have been developed despite of the difficulties and challenges in growing germanium on silicon substrates. Among them, there are devices of primary responsivity like p-n junction photodiodes [13-18], p-i-n photodiodes [19-25], and metal-semiconductor-metal (MSM) photodetectors [26-29] and devices with gain including avalanche photodiodes (APDs) [30][31] and MOSFET phototransistors [32].

The p-n junction or p-i-n junction photodiodes are simplest in device structure and physics. For germanium-on-silicon or germanium-on-SOI substrates, the active junctions are usually all in germanium to exclude the very defective Ge/Si interface [16][20][21][24]. Some growth methods involve growing a thin buffer germanium layer first and confining all misfit dislocations within the thin buffer layer [33]. Then the germanium film grown homogeneously on top of the buffer layer is almost free of defects. Most other methods [53-76] are also devoted to improve the bulk germanium but very little attention is paid to optimize the Ge/Si interface. With these techniques, normal incidence p-i-n germanium photodiodes were demonstrated with responsivities as high as 0.89 and 0.75 A/W at 1.3 μm and 1.55 μm with response time <200ps [18]. Nonetheless, researchers have also built diodes on Ge/Si heterojunction [13][14] with optimized interface quality (effective diffusion length of 20-30nm [34]) and hence decent responsivity (16 and 5mA/W at 1.3 μm and 1.55 μm [14], respectively). The p-i-n photodetectors can usually be very fast too. A large bandwidth of 39GHz was achieved in

normal incidence p-i-n diodes realized by Ge grown on Si by molecular beam epitaxy [20][21]. Even with the constraints of the growth being CMOS-compatible and the device being monolithically integratable, high responsivity Ge on Si p-i-n photodiodes were demonstrated which can be operated at 10Gbits/s [23]. To overcome the efficiency-bandwidth trade-off which is usually encountered in p-i-n or p-n junction diodes, waveguide photodetectors [15-17][25] can be used to decouple light absorption and photocarrier drift directions which allows for independent optimization of absorption on one side and collection efficiency and speed on the other (Fig. 1-4). With this waveguide configuration, Masini et al. demonstrated a CMOS-compatible Ge waveguide photodetectors with 0.85 A/W responsivity at 1V reverse bias and with speed in excess of 20GHz [15].

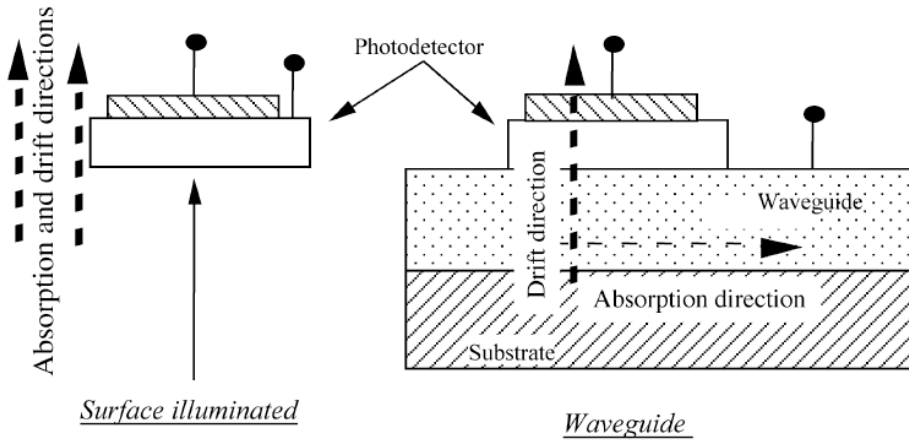


Fig. 1-4 absorption and drift directions are decoupled in a waveguide photodetector allowing for independent optimization of efficiency and speed (reproduced from ref. [16]).

Since chip-level optical interconnects require high-speed and low-capacitance photodetectors, the active regions of photodetectors need to be made very small, i.e. subwavelength. But with a subwavelength active region, the coupling efficiency of light to and hence the absorption efficiency of the active region would be very poor. Nanometallic focusing structures (e.g. C-shaped nanoaperture [35] and dipole antenna [36]) were therefore built around the tiny detectors to enhance the optical near field to significantly improve its responsivity as well as speed. However, p-i-n photodiodes usually have relatively large capacitance which limits high-speed operation and raises energy requirements in the chip-level interconnect systems.

Among photodiode structures, metal-semiconductor-metal (MSM) photodiode is considered one of the most promising candidates for receiver optoelectronic integrated circuits due to its ease of integration with preamplifier circuits, low detector capacitance, and large device bandwidth. But the problem with MSMs made on Ge and Si is high dark

current associated with a lower bandgap of the semiconductor, which leads to extra power consumption. The scheme of asymmetric electrode design was introduced and has proved to effectively suppress the leakage in MSM photodetectors [29].

Germanium avalanche photodetectors (APDs) using charge amplification close to avalanche breakdown, can achieve high gain and detect low-power optical signals, so they can be candidates of the photodetector in chip-scale optical interconnects. But Ge APDs are universally considered to suffer from an intolerably high amplification noise [37]. Although by using separate silicon layer for amplification and germanium layer only for detection of light signal, high gain with low excess noise has been demonstrated [31], the relatively thick semiconductor layers limit APD speeds to about 10GHz and in the meantime require excessively high bias voltage of around 25V. However, researchers at IBM T. J. Watson Research Center recently demonstrated a germanium waveguide-integrated APD [30] (Fig.1-5), in which by shaping the electrical field on nanometer-scale they dramatically reduced the amplification noise by over 70%. With nanophotonic and nanoelectronic engineering, strongly non-uniform electric fields is generated in metal(W)-germanium-metal diodes so that the region of high electrical field for impact ionization in germanium is reduced to just 30nm at the vicinity of the tungsten plug. This extremely small region of avalanche multiplication benefits the device with dramatic reduction of noise, mainly for the reason that the thin gain region favors a “more deterministic statistics of ionization process” and “a narrower ionization-path-length probability distribution function”. Furthermore, this Ge APD of very small size only needs a bias voltage of only 1.5V to achieve an avalanche gain of over 10dB with operational speeds greater than 30GHz. The resulting bandwidth-gain product of 300 is among the highest ever reported for APD photodetectors. Although this reinvention of Ge APDs seems to solve some major problems of avalanche photodetector, they still suffer from inherent reliability and thermal issues.

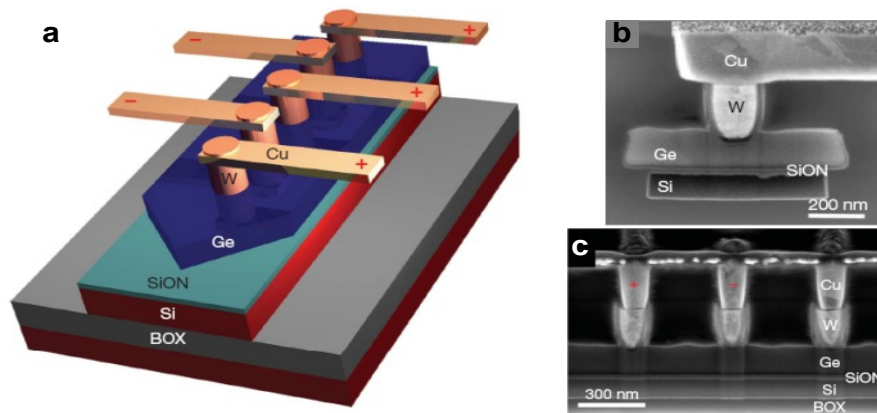


Fig. 1-5 Ge waveguide-integrated APD (a) Schematic; (b) SEM image of lateral cross-section; (c) SEM image of longitudinal cross-section (reproduced from ref. [30]).

1.2.1 Phototransistors

Phototransistors are another form of photodetectors, besides APDs, that have internal gain added upon primary responsivity. Combining a detector and a transistor into one compact device is an excellent approach towards realizing the “receiverless” photodetector which is desired in chip-level optical interconnects. Such a device should be easily integrated into state-of-the-art transistor chips and can be readily scaled down as a transistor to obtain extremely low device capacitance. The additional gain mechanism, i.e. transistor gain, also helps to relieve the requirement on input light level which would otherwise be quite stringent with only primary photo- responsivity.

The concept of phototransistor was introduced shortly after the demonstration of the first transistor in 1947. However, it was Shockley et al. in their 1951 paper [38] who first proposed the idea of using the bipolar transistor configuration as a phototransistor, and afterwards, even various other types of transistors emerge, when people talk about “phototransistor”, unless otherwise specified, by default they mean the bipolar configuration. Shockley also pointed out that in the phototransistor photo-induced hole-electron pair generation replaces carrier injection by the emitter junction. Thus the base contact is usually left floating. The first demonstration of a phototransistor with the bipolar configuration was actually realized in germanium [39]. It was a homojunction phototransistor with gain or quantum yield of ~ 100 . The performance of the phototransistor was later found to be improved by using an emitter with wider bandgap than base. This idea of “wide-gap” emitter was first proposed by Shockley [40] and Kroemer [41].

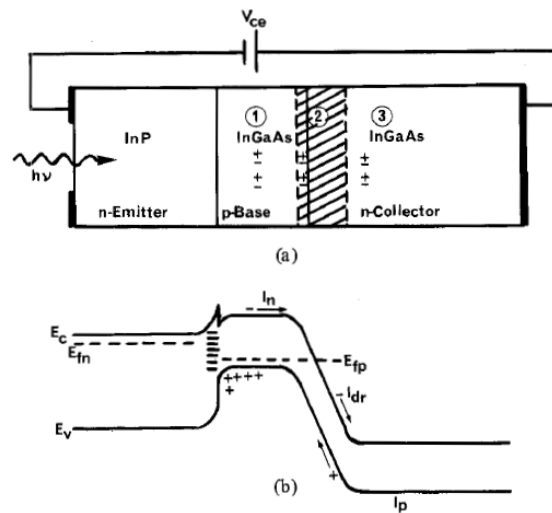


Fig. 1-6 Operation of a floating base HPT: Schematics of (a) cross-section view and (b) energy-band diagram (reproduced from ref. [42])

Fig.1-6 shows the schematics of a heterojunction n-p-n phototransistor (HPT) with a

floating gate and its energy-band diagram [42]. The InP emitter has a bandgap energy approximately 0.6 eV greater than that of the InGaAs base and collector. The emitter injection efficiencies close to unity can be achieved in the heterojunction transistor regardless of the relative base-emitter doping levels. Unlike homojunction transistors which require a lightly doped base and a heavily doped emitter for efficient injection from the emitter to the base, the barrier at emitter-base heterojunction of the HPTs alone can prevent reverse injection from the base. Hence a heavily doped base can be used to reduce the base resistance and a lightly-doped emitter can be utilized to decrease the base emitter capacitance. Light is incident through the transparent InP emitter and is absorbed primarily in the base region, although some absorption also occurs in the base-collector depletion region. The optically generated holes are trapped in the base region and the accumulation of excessive holes causes an increase in the forward bias of the emitter-base junction, or equivalently lowers the barrier for electrons to flow from emitter to base [43]. Current amplification is thus achieved by ordinary transistor action when the base width W_B is smaller than the electron diffusion length L_D in the base. The speed of a phototransistor is limited by the charging times of the emitter and collector [1]. So HPTs improve the speed over that of the homojunction ones with both smaller base resistance and less base-emitter capacitance. It was also found [44][45] that by adding a base terminal and with an optimally chosen external bias current, the phototransistor can run faster with enhanced optical gain.

In spite of all these improvements in performance, the gain-bandwidth products achieved of phototransistors were limited and never exceeded that of APDs. Also heterojunction phototransistors were considered too costly to be commercially feasible [1]. The research on phototransistors was then taken over by other photodetector technologies like APDs. However, now that with the ongoing research in chip-scale optical interconnects which asks for well-integrated “receiverless” photodetectors, there should be revived research interests on phototransistor. Furthermore, the improved capabilities of growing germanium on silicon wafers permits the HPTs to be built on Ge/Si hetero-stacks and thus solved problems with compound semiconductor (III-V) technologies which lack the vital cost-effective integration capacity with advanced Si VLSI technology.

Historically, photosensitive transistors with field-effect transistor (FET) configuration have also been the subjects of interest. These photo-FETs include PD-FET [46], MESFET [47] and MOSFET [32]. The advantages of this type of photo-transistors that combine high-impedance amplifiers with built-in photodetectors are believed to have very fast response and high optical gain. However, there have been some debates over the origin of gain observed in these FETs [47][48]. Various experimental evidences indicate that the gain in FETs can actually be a complicated combination of several mechanisms, including photoconductivity gain [47], transconductance gain due to the photovoltaic response of the gate or the substrate-channel junction [48], and the channel conductance

modulation due to field screening by the generated photocarriers [46][32].

1.3 Proposal of Photo-Hetero-JFETs

In our effort to create a technology of photodetectors to accelerate the advance of chip-level optical interconnects, we proposed a type of germanium photodetector with the field-effect transistor configuration [49]. The device structure is presented in Fig. 1-7, which integrates a Ge/Si heterojunction photodiode with a field-effect transistor. In other words, it is essentially a junction-field-effect transistor with a floating photosensitive germanium gate. In this photosensitive JFET, incident near-infrared light replaces the traditional electrical gate voltage to modulate channel conductance and thus turn the JFET on. The device is therefore named as Photo-Hetero-JFET.

Obviously Photo-Hetero-JFET can be seamlessly integrated onto silicon chips and can be scaled down with the silicon technology to obtain an extremely small capacitance. Secondary gain added to primary photoresponsivity further enhances photosensitivity of the device which helps to relieve the otherwise stringent requirement on the input optical power. Another advantage of this device is that with no electrical wires connecting the gate the photodetector capacitance is not limited by the non-scalable wire capacitance.

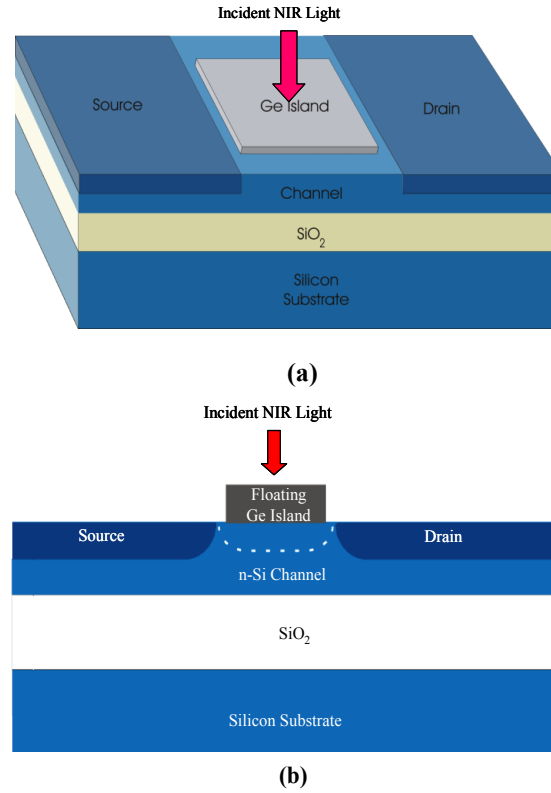


Fig.1-7 Device structure of Ge/Si Photo-Hetero-JFET (a) three-dimensional view (b) cross-sectional view

Near-infrared light can be coupled to the photosensitive germanium gate at normal incidence as shown in Fig. 1-7. That's how the Photo-Hetero-JFETs are characterized in our lab setting (you may refer to Chapter 4 for details of the experimental set-up). When the photodetector is built onto chip, light can then be coupled to the germanium mesa through a silicon waveguide. Fig. 1-8 shows a possible configuration of routing light signal through waveguide and sending it to the Photo-Hetero-JFET, with both the waveguide and the photodetector built on an SOI platform. An array of holes with periodic spacing is etched at the end of the waveguide to form one-dimensional photonic crystal reflector. With the same reflector placed on the other side of the photodetector, the light coupling efficiency can be greatly enhanced. This cavity-enhanced configuration is useful in counteracting the poor coupling efficiency when the germanium gate is scaled to an extremely small size for lowest capacitance.

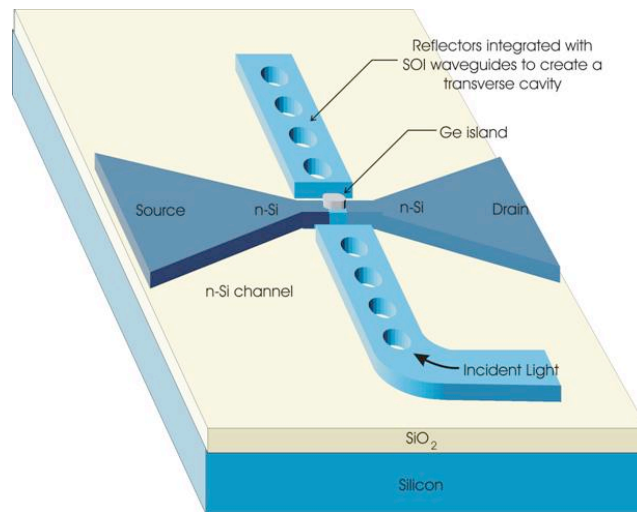


Fig. 1-8 Photo-Hetero-JFET in waveguide-coupled and cavity-enhanced configuration

1.4 Organization of this dissertation

This chapter gave the introduction to the background and the motivation of this thesis work. It looked at the limitations of electrical interconnects in chip-to-chip and on-chip communications, and introduced optical links as a most promising candidate for replacement. It then discussed the technological challenges of the chip-scale optical interconnect with a focus on its receiving end. The conclusion is that the photodetectors in the chip-level optical interconnect should be *highly-integrated* and have *extremely small device capacitance*. This chapter reviewed the various types of photodetectors including phototransistors, which finally lead to the proposal of the subject of this thesis work, Ge/Si Photo-Hetero-JFETs.

Chapter 2 looks at design issues and operating mechanisms of Photo-Hetero-JFETs. It starts from the basics of Ge/Si heterojunction by looking at heterogeneous growth of Ge on Si, and mechanism of photovoltaic response in the Ge/Si heterojunction. Based upon that, it then discusses the design of the Photo-Hetero-JFETs including its device structure and operating principles.

Chapter 3 looks at the fabrication of both heterojunction diode devices and Photo-Hetero-JFETs in great details. It describes the challenges in fabricating the nano-gate phototransistor and techniques exploited in tackling them.

Chapter 4 is devoted to the experimental characterization and analysis of the Photo-Hetero-JFETs that has been fabricated. Both steady-state and time-resolved transient response of Photo-Hetero-JFETs are obtained and analyzed. It also looks at the performance of heterojunction diodes both under continuous-wave and pulsed illumination, which provides very important physical insights in understanding the performance of the hetero-JFET device. Different models are attempted in analyzing the device, and it is found that the poor germanium material quality may have severely limited the quantum efficiency and slowed the gain.

Chapter 5 proposes future work in improving the Photo-Hetero-JFETs. It also looks into other possible types of germanium photosensitive transistors with potentially great sensitivity before it concludes this dissertation.

Chapter 2 Design Issues of Photo-Hetero-JFET

As described in the previous chapter, the Photo-Hetero-JFET is based on a silicon JFET structure, with a germanium floating gate absorbing near-infrared light and hence modulating the silicon channel conductance. Therefore, in this photonic “junction field-effect transistor”, the germanium/silicon heterojunction is where all interesting physics of this Photo-Hetero-JFET happens. This chapter will start from the fundamentals of Ge/Si heterojunction, then explore the operating principles, and from there, discuss the design issues of the JFET phototransistor.

2.1 Fundamentals of Ge/Si Heterojunction

2.1.1 Issues about Ge growth on Si: challenges and approaches

The first challenge of integrating Ge with Si is the difficulty of epitaxially growing germanium on silicon, which comes from the 4% mismatch between their lattice parameters. This large difference in their lattice constants severely limits the thickness of the pure defectless germanium film that can be grown on silicon substrate.

During the heteroepitaxy process, the first Ge layer deposited aligns its atoms to those of silicon substrate. This creates compressive strain in Ge along the growth plane and tensile strain along the normal plane. Such strain is accumulated during the following epitaxial growth until the distorted energy is big enough to relax the film through inserting misfit dislocations - usually extra planes of atoms. This occurs when the film reaches the thickness defined as the “critical thickness” [50]. These misfit dislocations are confined to the interface of the epilayer and the substrate, and are energetically stable even after the critical thickness is reached. However, the more detrimental dislocations in the epitaxial film, in terms of their effects on device performance, are threading dislocations. They are the byproduct of the misfit dislocation formation and typically thread from epi-substrate interface to epilayer surface, as dislocations cannot end in a crystal and have to either form a loop or terminate at a free surface [1]. These dislocations are sites for carrier recombination which results in reduced responsivity and large leakage currents in photodetectors. Apart from introducing large density of dislocations in the device film, accumulated strain during growth also energetically favors 3-D island formation at surface [50] instead of layer by layer growth, leading to high surface roughness, which may cause difficulty in process integration.

Owing to the 4% lattice mismatch of the Ge/Si system, the critical thickness of pure Ge epitaxially grown on Si substrate is shown to be only around 10\AA [51][52]. Given the absorption length of near infrared light in pure germanium being a few microns [13], any

germanium photodetectors of practical use would have device layer much thicker than the critical thickness and with low density of dislocations.

There have been many reported techniques of obtaining germanium epilayers of good quality on silicon substrate [53-77]. These novel approaches have resulted in threading dislocation densities in the range of $10^7 - 10^9 \text{ cm}^{-2}$, and have enabled the realization of efficient germanium photodetectors as well as germanium transistors. Some of the important works and techniques are summarized in the following to show the extensive efforts put and successes achieved in this field.

The method of **graded buffer layers** was demonstrated by Fitzgerald *et al.* [53-55]. They grew SiGe relaxed graded buffer layers on Si at high temperature, and showed that high quality relaxed epilayers with Ge content from 0-100% can be grown. By staying within the low mismatch region with the introduction of each grading layer, they only introduced a small number of new dislocations which prevents massive dislocation nucleation, interaction and multiplication events that would otherwise increase threading dislocation density. In addition, the low mismatched layer grown provides the strain to glide dislocations out of the edge of the substrate. This graded buffer technique, together with an intermediate Chemical Mechanical Polishing (CMP) step, was able to reduce the threading dislocation density in the final Ge film to a record value of $<2 \times 10^6 \text{ cm}^{-2}$. Instead of relaxed graded buffer layers, Luryi *et al.* used strained **superlattice buffer layers**, each within critical thickness, to minimize the insertion of dislocations [56]. It is believed that strain can also act as a barrier to the vertical movement of threading dislocations. With the technique of superlattice buffer layers, they successfully demonstrated p-i-n germanium detectors on silicon with a quantum efficiency of 40% at 1300nm [56]. Researchers also reported the method of **low temperature Si buffer layer** [57-61]. They demonstrated dramatic reduction of the threading dislocation density in the SiGe layer after the insertion of a low-temperature MBE grown silicon buffer. The suggested mechanism for this improvement is that point defects in the silicon buffer layer can trap the dislocations [62].

A **very high temperature MBE** process (at 900°C) was utilized by Malta and his co-workers to achieve localized germanium melting and alloying with silicon, thereby confining extensive threading dislocations near the Ge/Si interface [63]. Etch pit density measurements on the germanium films showed that the dislocation density in Ge bulk away from the epi/substrate interface was as low as 10^5 cm^{-2} .

Various thermal treatments are also used to anneal out defects and thus reduce dislocation density. After growing a thin germanium buffer layer followed by thick layer at elevated temperature, Kimerling *et al.* subjected the film to **cyclic temperature annealing** treatment. With that, they have built p-i-n photodetectors on 4μm germanium layers on

silicon, which showed responsivity of 0.89A/W at 1300nm [64]. **Multiple Hydrogen Annealing for Heteroepitaxy (MHAH)** is another thermal treatment technique introduced to grow high quality pure germanium on silicon with low threading dislocation density [65,66]. In this technique, in-situ annealing is carried out at a higher temperature in an H₂ ambient after a thin germanium buffer layer is first grown heteroepitaxially on silicon. Such annealing is shown to reduce the surface roughness by 90% and relieve stress in the first few tens of nanometers. After that, more germanium is then grown homoepitaxially on this virtual germanium lattice with no introduction of defects. Okyay *et al.* have used this technique to grow germanium and fabricated an integrated germanium photodetectors on silicon [1]. They've obtained 50× reduction in threading dislocation density with final density of $1.5 \times 10^7 \text{cm}^{-2}$.

Selective growth has been shown to effectively reduce the overall threading dislocation density, because small patterned area growth reduces dislocation density and hence dislocation interactions [67,68], as well as reduces the distance the threading dislocations need to travel before they reach the sides of the epilayer [69,70]. **Epitaxial lateral overgrowth** using **nanoscale Ge seeds** even enables germanium growth over SiO₂ film [71]. Those 7-nm-wide seed pads form in the oxide layer when exposed to a germanium molecular beam and they then “touchdown” on the underlying Si. Further exposure to the molecular beam makes germanium selective growth on the seeds which later on coalesce to form an epitaxial lateral overgrowth (ELO) layer. The ELO layer should be free of dislocation except that stacking faults exist at Ge-SiO₂ interface.

One different perspective was put-forward suggesting that instead of trying so hard to reduce the threading dislocation density, one can route the dislocations to thread into the substrate rather than into the epilayer so as to obtain dislocation-free epi-films. By using thin **compliant substrates**, researchers have grown epilayers with very low threading dislocation densities [72-76].

One might have noticed that, most of the techniques reviewed here so far have not paid additional attention to reduce the dislocation density near or at Ge-Si interface. Some of them even sacrifice the material quality at the epi-substrate interface, confining most threading dislocations there, in order to obtain dislocation-free “bulk” part. Unfortunately, in our design of Photo-Hetero-JFET, not only the “bulk” part of the germanium film, but also that near the interface is required to have low dislocation density. In addition, the material quality of the silicon substrate or the silicon layer of SOI substrate where germanium film is grown on should not be compromised either. Therefore, techniques that utilize buffer layers or compliant substrates, or involve localized germanium melting/annealing, are not applicable in the material growth/preparation for our photodetector.

One attempt to improve the material quality of the entire heteroepitaxial germanium layer is to **optimize the substrate cleaning/preparation recipe** prior to the epitaxial growth. Subal *et al.* showed that [77] the best epi Ge film is obtained by finishing the silicon substrate cleaning with Piranha, which ensures that the Si surface ends up being terminated by oxide when introduced into the MBE chamber. The oxide is then desorbed using a high temperature in-situ annealing at 800°C. They believed that following this oxide-removal technique results in “the cleanest possible Si surface for epitaxy”. Their gauge of the germanium epilayer quality is the minority carrier diffusion length L_D in the film near epi-substrate interface, which can be estimated by measuring photoresponsivity of the Ge/Si heterojunction. It has been accepted that this minority carrier diffusion length L_D , independent of the device geometry and experimental methods, is an intrinsic measure of semiconductor material in the applications of electrons or optoelectronics, unless the material is so defective that geminate recombination dominates. The diffusion lengths for their best MBE samples that are subjected to the optimized substrate preparation and growth conditions are ~60nm [77].

Masini *et al.* showed that they could build Ge/Si heterojunction photodiodes with uncompromised responsivity out of polycrystalline germanium thermally evaporated on silicon [13]. The diffusion length in their poly-Ge film was reported to be in the range of 20-30nm. Their thermal evaporation of germanium is carried out in a vacuum chamber with a background pressure of 1e-6 Torr, using grains of 99.999% pure Ge source, with Si substrate held at 300°C. Prior to evaporation, Si substrate goes through a preclean in HF acid and a rinse in DI water. Raman spectroscopy, shown in Fig. 2-1, demonstrates that Ge films undergo the transition from amorphous to polycrystalline as the substrate temperature exceeds 250°C and the amorphous phase vanishes above 300°C. They also show that the absorption spectrum of polycrystalline Ge is quite similar to that of the crystalline Ge [13] (see Fig. 2-2). However, polycrystalline germanium would obviously have worse carrier mobilities and lifetimes than those in single crystal Ge.

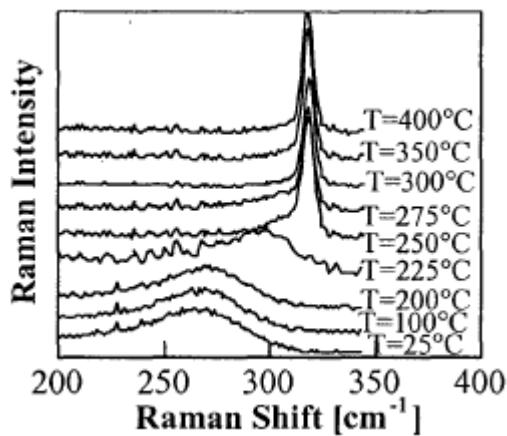


Fig. 2-1 Raman spectra of Ge films evaporated at different temperature [13].

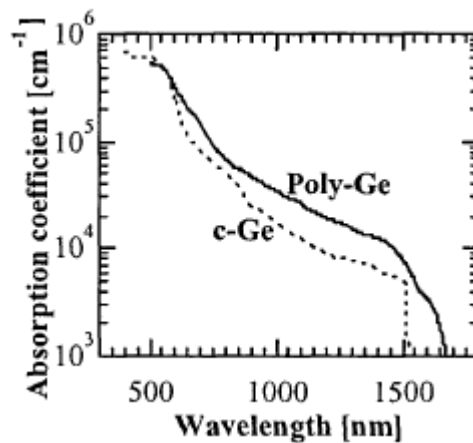


Fig. 2-2 Absorption spectra of poly-Ge (solid line) and crystalline Ge (dashed line) [13].

Our preliminary results of Photo-Hetero-JFETs was actually obtained on proof-of-concept devices fabricated on the single-crystalline Ge films grown on SOI substrates with the same MBE process as the best film with diffusion length of 60nm had gone through. The diffusion length in the germanium film grown on these SOI wafers was not as spectacular, only 8-10nm, which we attributed to the damage of the substrate surface caused by the ion implantation step in the attempt to make the silicon device layer n-type. We later started to cooperate with Masini's group in getting germanium layers grown on SOI wafers. This time we've learned our lesson and avoided the ion implantation step, leaving the top silicon layer as it is, which is p⁻-type or almost intrinsic. The best germanium films that we've obtained showed very small diffusion length values (~1-2nm) through responsivity measurements of the heterojunction diodes made out of them. We've realized at a much later stage of this thesis work, that diffusion length may no longer be a valid picture; instead, geminate recombination which researchers have studied in amorphous materials for solar cells [79, 80] fits better. Since the thermally-evaporated germanium films were the best accessible material for us at the time, the nano-gate Photo-Hetero-JFET devices and p-n junction photodetector devices that this thesis work discusses on in the remaining chapters are all fabricated out of them. The reason that we go into this length in this chapter reviewing and discussing hetero-growth of germanium on silicon substrate is that the poor material quality turns out to be the most important limiting factor that prevents our photo-JFET detectors to be ultra-sensitive, which will reveal itself in later chapters.

2.1.2 Band Structure of Ge/Si Heterojunction

Despite all the efforts that researchers have made in reducing the dislocation density, due to the inherent large lattice mismatch, hetero-grown pure germanium films are usually still quite defective, especially near the Ge/Si interface. Those defects in the germanium film, which take the form of isolated dislocations, introduce deep electronic states in the bandgap, pinning Fermi level close to valence band edge. Furthermore, lattice mismatch between Si and Ge leaves roughly 8% of the Si surface atoms with dangling bonds. Although no dopants are intentionally incorporated during the film growth, Ge film normally exhibits p-type characteristics with peak doping at the interface approaching 10^{18}cm^{-3} . According to Di Gaspare *et al.* [78] energy gap difference between Si and Ge are accounted by a valence band discontinuity of 0.36eV and a conduction band discontinuity of 0.1eV. The resultant band alignment for p-Ge/n-Si is shown in Fig. 2-3. Since the doping level in Ge is very high, especially at the interface, and the Si layer is desired to have moderate doping level ($10^{15} - 10^{16}\text{cm}^{-3}$), there is negligible depletion in Ge, and the depletion region is almost all in Si.

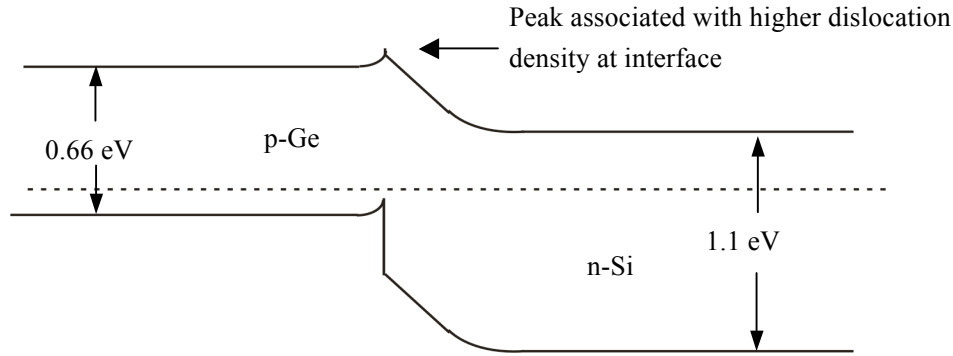


Fig. 2-3 Band structure of p-Ge/n-Si heterojunction

2.1.3 Photocarrier Separation at Ge/Si Heterojunction

When near-infrared light is incident on the above heterojunction, it only generates electron-hole pairs in Ge because the bandgap of Si is bigger than the incident photon energy. As there is no depletion region in Ge film, there's no built-in electric field there to assist transport of generated photocarriers or to separate them. Hence, the carrier transport in germanium is solely by diffusion. Photocarriers that can survive from recombination and diffuse to the Ge/Si interface can see the built-in electric field in Si and then get separated. In an average sense, only photocarriers generated within one diffusion length near the interface can be collected as useful photocurrents. That's why diffusion length in germanium is associated with responsivity or quantum efficiency of a Ge/Si heterojunction diode. Although lack of field-assisted carrier transport in germanium is not at all beneficial for carrier collection, the band-alignment of Ge/Si heterojunction conveniently facilitates carrier separation. When electron-hole pairs diffuse to the Ge/Si interface, photo-electrons merrily drift down the potential slope of the conduction band into the silicon side while photo-holes see the potential barrier of the valence band and are left behind in Ge. Charge separation is therefore achieved (See Fig.2-4). The photo-electrons that go to the silicon side neutralize the ionized donors in the depletion region and decrease the depletion width. Or, in a solar-cell model, the separation of photocarriers causes quasi Fermi-level separation as if a forward bias V_F is applied across the junction. These two physical pictures, depletion-charge model and solar-cell model, should be essentially equivalent. They are the basis on which the proposed Photo-Hetero-JFET is designed and modeled.

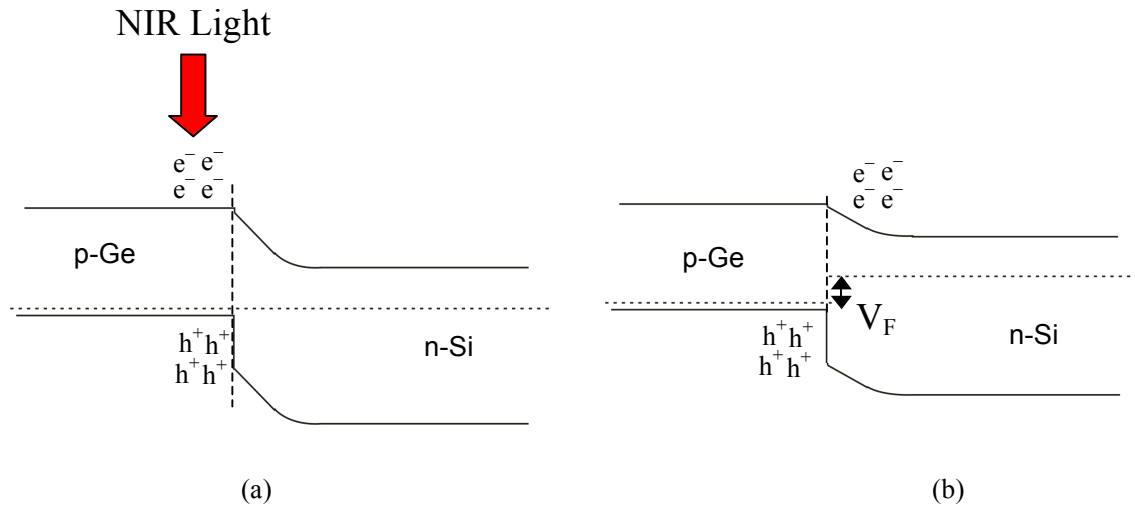


Fig. 2-4 (a) Incident IR light creates electron-hole pairs in the Germanium (b) The electrons diffuse into the Silicon, creating charge separation. This forward biases the open junction by an amount V_F that depends on the amount of charge separation (reproduced from ref. [77]).

It is evident from the heterojunction band-alignment that lightly doped n-type Si is preferred over the lightly doped p-type Si in the Ge/Si heterojunction. Because Si has a bandgap that is inherently larger than Ge, even lightly doped p-type Si, when forming the heterojunction with Ge, will result in an uphill conduction band slope (see Fig. 2-5), which impedes the photo-electrons to diffusion over. That's the reason, for sample materials used for the proof-of-concept devices, p-SOI wafers were ion implanted into n-type before single-crystalline germanium was grown by MBE.

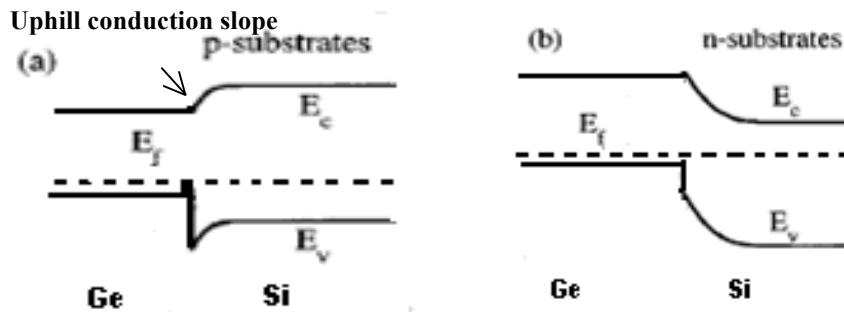


Fig. 2-5 Band-diagrams of Ge/Si heterojunction with p-Ge on (a) p⁻-Si substrate with resistivity of 13.5-22.5 $\Omega\cdot\text{cm}$ (spec of SOI from SOITEC), and (b) n⁻-Si substrate with n-type dopants of density $2.5\times 10^{16}\text{cm}^{-3}$.

2.1.4 Quantum Efficiency and Diffusion Length

From the discussion of the previous paragraphs, we know that in p-Ge/n-Si heterojunctions subjected to near-infrared light, it is the electron diffusion length in germanium that determines the fraction of photocarriers that can be collected efficiently. Evidently, the longer the diffusion length is, the larger the percentage of photocarriers collected resulting in better responsivity. Responsivity is heavily structure-dependent and often involves the effects of other external factors including light coupling efficiency. Differently, diffusion length is only material-dependent, and it ultimately limits the responsivity or quantum efficiency that any device structure made out of this material can achieve. This picture presented below shows that photo-electrons within one diffusion length from the junction interface are collected by the built-in electric field in the Si.

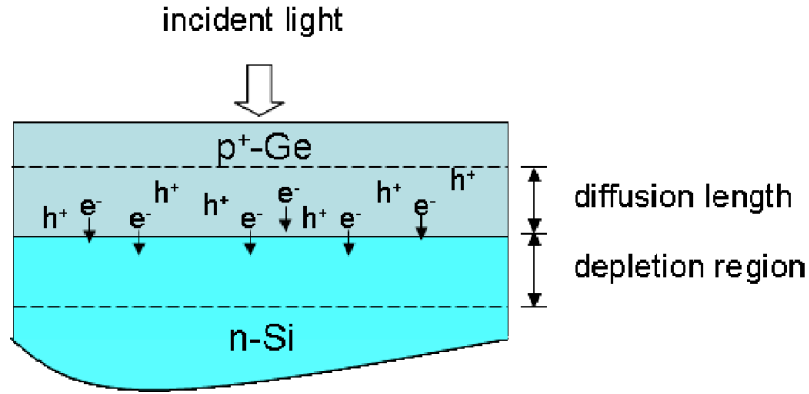


Fig. 2-6 Diffusion length and depletion region in p-Ge/n-Si heterojunction

So, if the incident light power is P_0 , the absorption coefficient of Ge is α , the minority carrier diffusion length is L_D and the reflectivity of air/Ge interface is r , for top illumination on the diode structure shown in Fig. 2-6, the responsivity is

$$R = \frac{I}{P_0} = \frac{P_0}{P_0} \frac{q(1-r)\alpha L_D}{hv} = \frac{q}{hv} (1-r)\alpha L_D$$

The quantum efficiency of this diode structure, which describes the ratio of number of photoelectrons that contribute to photocurrent to the number of photons incident, is then

$$\eta = \frac{hv}{q} \cdot R = (1-r)\alpha L_D$$

Thus, electron diffusion length in p-Ge can be extracted from responsivity measurement done on p-Ge/n-Si heterojunctions as shown in the following equation.

$$L_D = \frac{hv}{q} \cdot \frac{R}{(1-r)\alpha} \quad (2.1)$$

The material samples that we used to fabricate our devices were characterized in this way.

Simple p-Ge/n-Si heterojunction diodes were fabricated similar to the diode structure shown in Fig.2-6. Responsivity measurements were then carried out and diffusion lengths are extracted. The fabrication and characterization of this heterojunction will be discussed in the later chapters. It is evident that heterogeneously-grown germanium films with longer diffusion lengths are desired, for the reason that it results in better responsivity that can be exploited from this device.

2.1.5 Geminate Recombination

In most semiconductor material with the quality to make useful optoelectronics devices, the diffusion length picture suffices to indicate the best quantum efficiency that this material can offer. This is due to the common belief that in single crystalline or poly crystalline semiconductor of decent material quality, the initial separation of photoinduced electron-hole pairs is very effective. However, in more disordered material systems, like amorphous semiconductor, this assumption of complete separation of photoelectron-hole pairs at its initial stage after being generated is not valid. One often has to include geminate recombination[79,80], which describes the recombination of an electron-hole pair dissociated from a parent exciton before obvious diffusion occurs, and in some cases one has to include the phenomenon that the “initial charge separation that converts an exciton to a bounded electron-hole pairs” even fails to occur. The possibility of such initial recombination was pointed out by Rutherford long ago [81].

However, the term of geminate recombination was first introduced in chemistry. It refers to the reaction, with each other, of two transient species produced from a common precursor in solution [82]. If reaction occurs before any separation by diffusion has occurred, this is termed primary geminate recombination. If the mutually reactive entities have been separated, and come together by diffusion, this is termed secondary geminate recombination. Later on, researchers working on organic or amorphous semiconductor solar cells borrowed this concept [79,80]. Primary geminate recombination in this context refers to the very initial recombination that prevents the dissociation of an exciton, and secondary geminate recombination corresponds to the recombination of the dissociated electron-hole pairs after some separation by diffusion. Since the recombined electron and hole should be from the same parent exciton, they really haven't diffused much to meet with other electrons or holes excited by different photons, and to recombine with them. Therefore, a bulk diffusion-length model cannot be used to describe geminate recombination in disordered material. Another reason that a diffusion-length model might not apply is that the transport of charged carriers in the semiconductor can be hopping conductance instead of continuous diffusion.

Geminate recombination, if not otherwise specified as primary, often refers to the secondary geminate recombination. Absorption of light leads to creation of excitons,

which may dissociate to form geminate, coulombically bound electron-hole pairs. These geminate pairs may in turn recombine, or separate from each other to become free charge carriers. The charge separation probability is determined by the ratio of the “intrinsic recombination” ratio to the sum of the electron and hole mobilities, k_0/μ [79]. In organic solar cells people had to assume exceedingly small values of k_0 to explain the poor charge separation probabilities, although some reported that the mobilities of charge carriers on ultrafast time scales are several orders of magnitude higher than their stationary value, which relaxed k_0 to reasonable values. The theory of geminate recombination [80] and its mathematic models [80][83] are certainly much more complicated and beyond the scope of this thesis work. However, it appears that in disordered material like amorphous semiconductor, geminate electron-hole recombination is one main factor limiting the quantum efficiency of optoelectronic devices that are built on it.

As mentioned in the previous section, the nano-gate Photo-Hetero-JFET devices are fabricated on germanium film thermally evaporated on SOI substrate. The germanium film was assumed to be “polycrystalline”, since the films that were grown under the same condition on silicon substrate are shown to be polycrystalline according to Raman Spectra (see Fig.2-1)[13]. However, while the silicon substrates are ensured to be held at 300°C when clamped to the heated holder, the surface temperature of SOI substrates with a buried oxide layer of 1 μ m can be much lower than the required temperature for the growth to stay in the polycrystalline phase regime. To characterize the material quality of the evaporated germanium film on SOI, responsivity measurements were done on heterojunction diode devices and the diffusion length was extracted to be ~1nm. This diffusion length value is indeed significantly smaller than the reported diffusion length (20-30nm) [34] in the evaporated germanium film on silicon substrate, which suggests that the germanium films on SOI have much poorer quality and could be amorphous. Furthermore, the estimated diffusion length of the germanium film on SOI is too short to be realistic. It will be shown in the later chapter that the worst possible diffusion length is ~1nm. A diffusion length of this extremely small value suggests that physically the carriers simply recombine at where they are generated – there’s not really any diffusion. Therefore, as we shall also emphasize in the later chapter, the quantum efficiency of photodetectors made on this evaporated germanium films on SOI substrates is better explained by geminate recombination instead of the diffusion length model. Nonetheless, for the previous proof-of-concept devices that are made of single-crystalline MBE-grown germanium films [49,77], their quantum efficiency can still be well-explained in terms of diffusion length.

2.2 Design of Photo-Hetero-JFET

2.2.1 Device structure

A cross-section view of Photo-Hetero-JFET with charge-separation in the heterojunction shown is presented in Fig. 2-7. It is essentially a junction FET structure. The main idea is to have a three terminal device or a transistor under a Ge/Si heterojunction. This is an attempt to significantly enhance sensitivity by harvesting gain - transistor gain and/or photoconductivity gain - on the photo-signals generated across the heterojunction, from a decrease in depletion width or a forward photovoltage bias. In this junction FET, intended to work as a photodetector, a germanium island is placed on the channel of a typical Si FET, functioning as a floating gate that controls the conductance of the channel. Note that, being different from traditional p-i-n or p-n junction photodetector design, there's no electrical contact on the Ge.

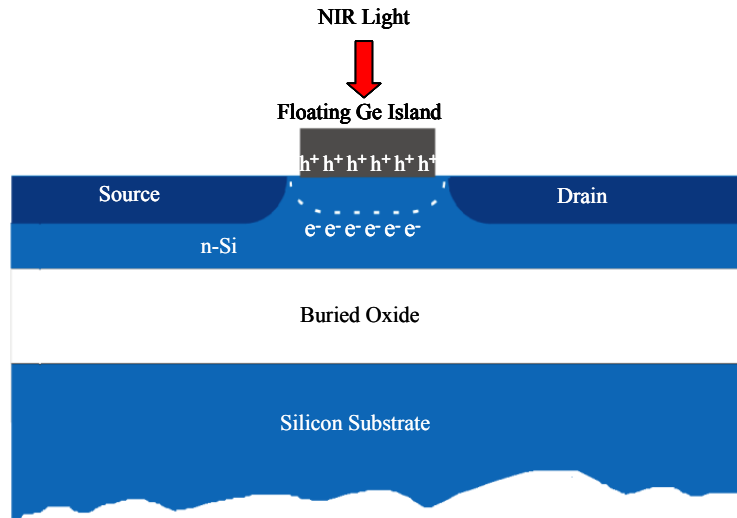


Fig. 2-7 Cross-sectional diagram of the proposed hetero-JFET detector.

2.2.2 Operating Principles of Photo-Hetero-JFET

In the Photo-Hetero-JFET, instead of having electrical voltage on the gate to modulate the channel conductance, separation of photocarriers effectively forward biases the gate-channel junction; equivalently, photoelectrons that go into silicon neutralize some of the ionized donors and reduce the channel depletion. This bias reduces the depletion in the Si and opens up the channel. This resembles the operation of a regular 'enhancement' mode JFET transistor, in which the channel is initially depleted. The silicon device layers of the SOI substrates that we used are 200nm thick, which should be completely depleted if the self-doping concentration in Ge is 10^{18} cm^{-3} and if the doping concentration in Si is

$2.5 \times 10^{16} \text{ cm}^{-3}$.

Another equivalent operating mechanism in the Photo-Hetero-JFET is often referred to by experts in photoconductors as “secondary photoconductivity” [84]. Photoholes that are left behind and immobile in the germanium gate can attract electrons from source to the channel. With a source-to-drain bias applied across the channel, electrons move and current flows. When the lifetime of holes in the gate (τ_h), or “dwell” time of photo-holes in the context of dispersive transport as we refer to as in Chapter 4, is larger than the transit time of electrons across the channel (t_{tr}), a single photo-hole can result in more than one electron flowing into the contacts and collected as photocurrent. Therefore, this photoconductive gain (G_{ph}) is proportion to τ_h/t_{tr} . One way to increase the photoconductive gain is by reducing t_{tr} . This is another good reason that drives us to scale down the device, especially in terms of shortening channel length. The transconductance gain of a JFET transistor is also increased with decreased channel length.

Both mechanisms, transconductance gain and photoconductive gain, can exist in the operation of Photo-Hetero-JFETs. Sometimes it’s hard to distinguish one from the other. In the framework of a junction-FET, induced electrons from the electrostatic coupling of the “immobile” holes (or holes slowly hopping between traps) in the gate neutralize some of channel depletion and the electric field from the gate charge creates channel “conductance” (“transconductance”). Also, with a bias across the channel, those “immobile” primary holes in the gate can keep attracting secondary electrons to flow from source to drain for photoconductivity (“secondary conductivity”). Therefore, as further discussed in Chapter 4, JFET transistor gain and photoconductive gain are referring to the same physics that happens in the operation regime of the Photo-Hetero-JFETs.

Chapter 3 Fabrication of the Photo-Hetero-JFET

3.1 Material preparation

3.1.1 Substrate choice and preparation

The choice of device substrate is Silicon On Insulator (SOI) wafers for the reason that it provides a good platform for the later integration of other silicon photonic devices, for example silicon waveguides, with the photodetector. As already explained in the previous chapter, for a better collection efficiency of photo-carriers, the top silicon layer is desired to be n-type. However, the SOI wafers that we had access to were SOI wafers from SOITEC with top p⁻-Si device layer (at time of purchase, SOITEC only had in-stock SOI wafers with p⁻-type device layers and the lead-time for wafers with n-type was too long). Our old strategy was to ion implant the p⁻-Si device layer into n-Si before the high temperature MBE growth. The targeted doping concentration in silicon is $\sim 2.5 \times 10^{16} \text{cm}^{-3}$ for the channel layer to be just completely depleted. But we found out that the electron diffusion length was much shorter in the germanium film grown on silicon layer of the SOI wafer that had gone through the ion implantation step ($\sim 8\text{-}10\text{nm}$) than that in the germanium film grown on silicon substrate without ion implantation treatment (60nm)[77]. As we proposed earlier, the ion implantation step might have done damage to the surface layer of the growth substrate which deteriorated the quality of the epitaxial film. One other possible reason for the shorter diffusion length could be that, in SOI substrates, the temperature of the growth surface did not reach the assumed growth temperature (800°C). Nonetheless, when later we were planning to get germanium growth for the nano-gate Photo-Hetero-JFETs, we still wanted to avoid the ion implantation step to leave the growth substrate less of imperfections.

We came up with a scheme that can dope the top silicon layer without an ion implantation step. In the fabrication process of nano-gate Photo-Hetero-JFETs, a germanium gate of 100nm length is patterned. After that, heavily n-type doped source and drain are formed by a self-aligned ion implantation process. During ion implant, ions knock into the target at a specific angle. The ions are then scattered by nuclei in the target so they do not keep their trajectory along the direction that they are incident at. In practice, a dielectric layer is usually deposited on the crystalline substrate to make sure that the ions are randomized or get enough scattering to stop at desired range. Therefore, in selective-area ion implantation with a mask, ions can scatter to some length under the mask. This is called the lateral straggle of ions (see Fig.3-1)[85]. Such a phenomenon is normally disliked by device engineers who make extremely small MOSFET transistors with submicron channels. In the ion implantation step to create heavily doped source and drain with the channel, lateral straggle of implanted ions can affect or even invert the

channel doping. What makes it worse are the annealing steps following the ion implant which can drive the ions to diffuse further laterally. So device engineers use techniques like spacers and lightly-doped-drain LDDs to leave rooms for lateral straggle and to reduce its range.

However, someone's nightmare can be a blessing for others. It is exactly this lateral straggle of ions in the self-aligned source and drain ion implantation step that helps us to fortuitously dope the channel underneath the gate. As the silicon channel is initially very light p-type ($5 \times 10^{14} \text{ cm}^{-3}$), with a large ion dose to make heavily doped regions and the gate length being only 100nm, it is quite easy to invert the doping type and achieve a doping level of $2.5 \times 10^{16} \text{ cm}^{-3}$. The proper ion implantation parameters and annealing recipes are found out by process simulations to achieve the desired source, drain and channel doping profile. This will be described in greater detail in the following subsection where the process flow of Photo-Hetero-JFETs is introduced. So the SOI wafers that we sent out for germanium film were left as they were without n-type doping.

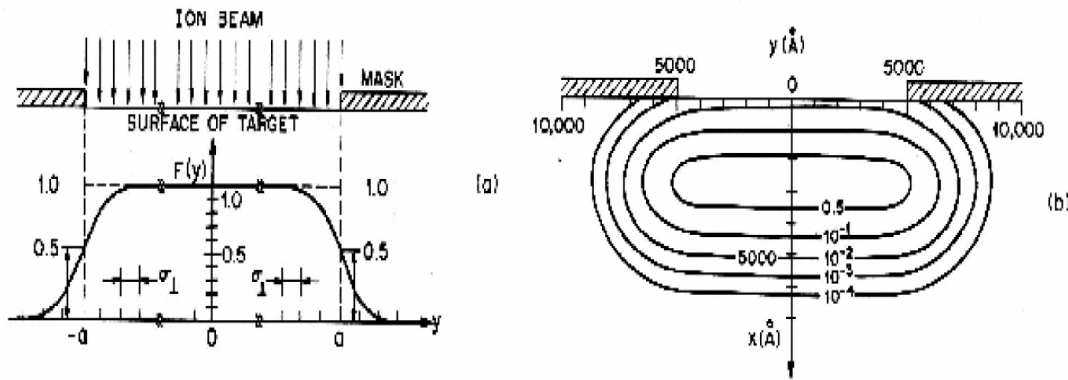


Fig. 3-1 Two-dimensional implantation profiles. (a) Fraction of total dose as a function of lateral position for an opaque mask. (b) Equi-concentration contours for a 70keV boron implant through a 1μm slit. (Reproduced from ref. [106]).

For germanium growth, we sought help from Masini's previous group [13,16] in Italy, who has demonstrated good work in depositing thermally evaporated polycrystalline germanium on silicon with decent diffusion lengths. They grew germanium films on the SOI substrates that we sent them using the following different combinations of substrate cleaning recipe and growth temperature listed in Table 3-1.

We characterized the germanium films they grew by performing responsivity measurements on the heterojunction diode devices fabricated out of them. The diodes that present the best responsivity are made on the germanium films grown in Run 111 and Run 112. It is expected that higher growth temperature helps the germanium atoms to become better registered to the substrates. Obviously substrates are cleaner with more

thorough removal of organic impurities by acetone. A rinse in 2% HF:H₂O following a 20s cleaning in BHF 1:7 does not help and even makes the situation worse. One possible reason is that with BHF cleaning, the growth silicon surface is passivated with H atoms and leads to a surface stable in air and a rinse in 2% HF:H₂O probably adds more H atoms upon that. However, this thin layer of H adatoms is believed to hinder the proper registration of germanium atoms with silicon substrate during the evaporation process [77]. To obtain a hydrogen-free surface, an in-situ annealing at >600°C is needed to completely desorb the H atoms. A higher substrate temperature can desorb H atoms more thoroughly which may be another reason why it results in better germanium films grown.

	substrate cleaning recipe	Growth temperature
Run 110	20s cleaning in BHF 1:7	300°C
Run 111	acetone rinse + 20s cleaning in BHF 1:7	300°C
Run 112	20s cleaning in BHF 1:7	490°C
Run 113	20s cleaning in BHF 1:7 followed by a rinse in 2% HF:H ₂ O	300°C
Run 114	20s cleaning in BHF 1:7 followed by a rinse in 2% HF:H ₂ O	490°C

Table 3-1 Different combinations of substrate cleaning recipe and growth temperature

3.2 Fabrication of heterojunction diode devices

P-Ge/Si heterojunction diode devices are made in order to characterize the germanium film grown, and more importantly, to understand the physics of its photoresponse in correlation with the mechanism of Photo-Hetero-JFET phototransistors.

The structure of the heterojunction diode is shown below in Fig.3-2. The material stack that we started from, to fabricate our devices is also indicative from Fig.3-2. The SOI substrate has a 200nm top p⁻-silicon device layer with resistivity of 14-22 Ω·cm sitting on a 1μm thick buried oxide layer (BOX). The thermally evaporated germanium film is 110nm thick.

The germanium mesa is 400μm×400μm in dimension, and was patterned by standard photolithography. Wet etching of germanium in CR-14 chrome etchant was used to obtain good selectivity over silicon. After that, contacts are made to the Si and p-Ge by e-beam evaporation at room temperature. Depositing Ti (2.5 nm)/Al (150 nm) on n-Si and Ag (300 nm) on Ge, gives the low contact resistance. Additional layers of Ti (5nm)/Au (100nm) are deposited on both contact metal stacks. The top gold layer is there to facilitate the gold wire bonding. Ti is again deposited as adhesion layer. The contact metal on Ge mesa is 160μm×160μm in size and is placed at one corner, leaving enough

window area for top illumination. A microscope picture of a die with finished devices is show in Fig.3-3. This die is then wire bonded to a chip carrier for optical and electrical testing.

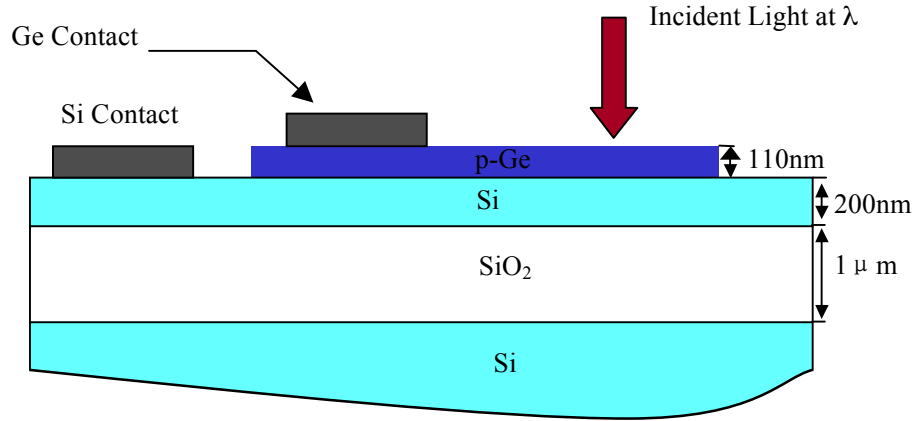


Fig.3-2 Cross-section of a p-Ge/Si heterojunction diode device

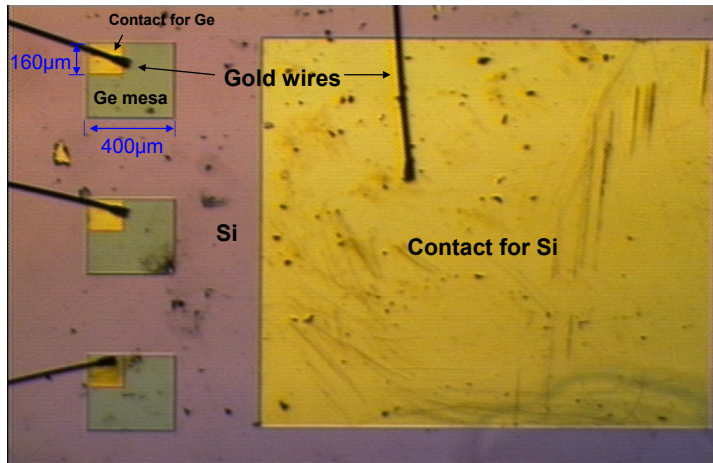


Fig.3-3 Microscope picture of a die with three finished heterojunction diode devices

3.3 Fabrication of Photo-Hetero-JFET devices

The first patches of Photo-Hetero-JFET devices were proof-of-concept devices that had channel lengths of 1 μm. As device performance (in terms of sensitivity and speed) gets improved with decreased channel lengths, the photodetector is then scaled down to have channel lengths (or gate length) of ~100nm. This section will be just focused on discussing the fabrication process of nano-gate Photo-Hetero-JFETs. Fig.3-4 - Fig.3-21 illustrates the various steps of the fabrication.

The material stack to start from is p⁻Ge (110nm)/Si (200nm)/SiO₂ (1 μm)/Si substrate,

which is shown in Fig. 3-4. Dies of roughly 1cm by 1cm are cleaved out of the wafer stack. The die is then cleaned in acetone, isopropyl alcohol (IPA) followed by DI water rinse. Stronger organic removers like Piranha can't be used, since a strong oxidizer like that reacts with germanium. In fact, germanium is very easily oxidized and chemically not as stable as silicon. Immediate exposure of fresh germanium in air will result in a thin layer of oxide which is easily soluble in water. Therefore, in handling dies with germanium films on, extra care has to be taken - DI water rinse in cleaning steps or developing steps are eliminated if it can be, and its encounter with strong oxidizers like some photoresist removers is avoided or minimized.

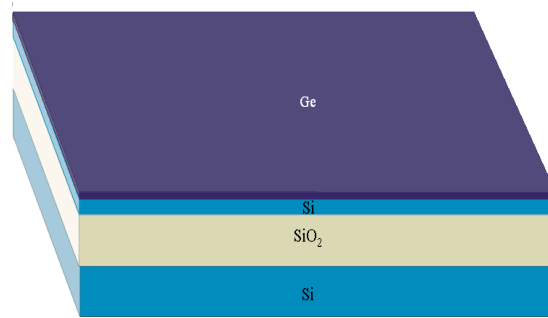


Fig.3-4 Material stack to start from: p-Ge (110nm)/Si (200nm)/SiO₂ (1μm)/Si substrate

3.3.1 STEP 1

Device mesas of 600μm×100μm are defined using standard lithography. The photoresist used in this photolithography step is AZ5214 E. This resist is intended for lift-off-techniques which call for a negative wall profile [86]. Normally a positive photoresist profile has a positive slope of 75 - 85° depending on the process conditions and the exposure equipment (only submicron-resist gets close to 90°). AZ5214E resist has image reversal capability and can result in a negative wall profile ideally suited for lift-off. However, AZ5214 is used as a normal IR photoresist here. Its positive slope of the patterned resist does not have big effects on the relatively large feature in the following etching step. A hard-bake of the patterned resist is done to improve the etch selectivity of the resist over the layers to be etched.

A 110nm Ge layer and a 200nm Si layer are etched all the way to the buried oxide in a Lam reactive ion etcher using Cl₂ and HBr mixture. The Lam etcher is the patented Transformer-Coupled-Plasma (TCP) system from Lam Research [87]. With TCP, a high density plasma can be generated even at low pressure (~12 mTorr) Also, a separate lower electrode is powered up at the same time with the upper TCP coil during the etch, so the plasma bias can be independently controlled. All this allows for creating deep submicron features with vertical etch profiles and high aspect ratios. Both Cl₂ and HBr etch Ge and

Si with good anisotropic and selective etching capability [88]. Cl_2 has higher etch rate while HBr provides better selectivity over oxide. Cl-based etchants have a lower purely chemical component. They can already produce byproducts with less volatility than F, and with stronger ion bombardment than F to increase the etch rate in the vertical direction. So they can achieve fairly anisotropic etching without a polymer inhibitor that is normally produced by adding H or C contents in F-based etchants. Moreover, with no polymer inhibitor layer that forms preferentially on silicon or germanium in Cl-based etching, the etch selectivity over oxide is better than that of F. Br-based etchants, in a similar fashion, can achieve even better anisotropy and selectivity over oxide. The ratio of Cl_2 and HBr in the mixture optimized for silicon etch in this Lam etcher is 50sccm:150sccm, and that for germanium etch is 100sccm:100sccm.

After the etch, the photoresist is removed in acetone. As mentioned earlier, stronger resist removers are avoided as they can oxidize Ge. The device structure after this step is shown in Fig.3-6.

Please note that rows of alignment marks (crosses made of $10\mu\text{m}\times 100\mu\text{m}$ bars) are also defined and etched with the device mesa. These alignment marks are to be used in the subsequent two electron beam lithography steps so that features are written at the correct locations of the mesa.

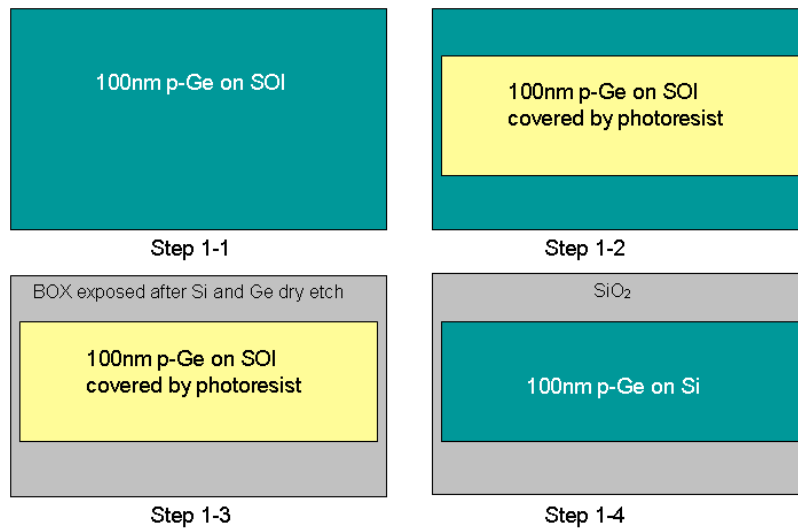


Fig.3-5 Top view of STEP 1 in making nano-gate Photo-Hetero-JFETs

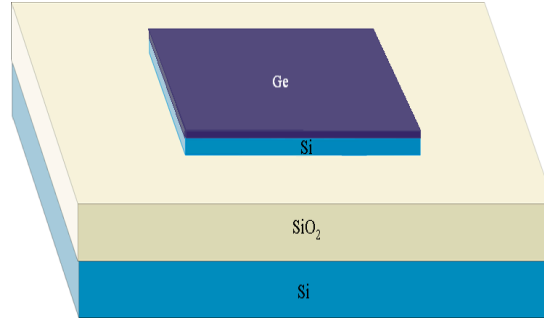


Fig. 3-6 Device structure after STEP 1

3.3.2 STEP 2

After the device mesas are formed, within each device mesa, a channel is created by isolating left part of the mesa from the right except for leaving a bridge between the two. Although the channel length aimed for Photo-Hetero-JFETs is 100nm, the length of the bridge is designed to be 1 μ m so as to leave enough margins for misalignment errors between two lithography steps. Since the source and drain regions of the FETs will be formed by masked ion implantation self-aligned to gate, they do not start at the ends of the bridge but at the edges of the gate to be patterned. Electron-beam lithography is used to define the bridge of 1 μ m or 2 μ m in length and 1 μ m in width. Positive ebeam resist PMMA (polymethyl methacrylate) 950 C4 is chosen since a resist with larger thickness (~500nm for PMMA 950 C4 spun at 3000rpm) is required for it to be an etch mask.

The same etch as described in STEP 1 is done to etch away Ge and Si uncovered by PMMA after the ebeam lithography step. After removing PMMA, the device mesa looks like what shown in Fig.3-8.

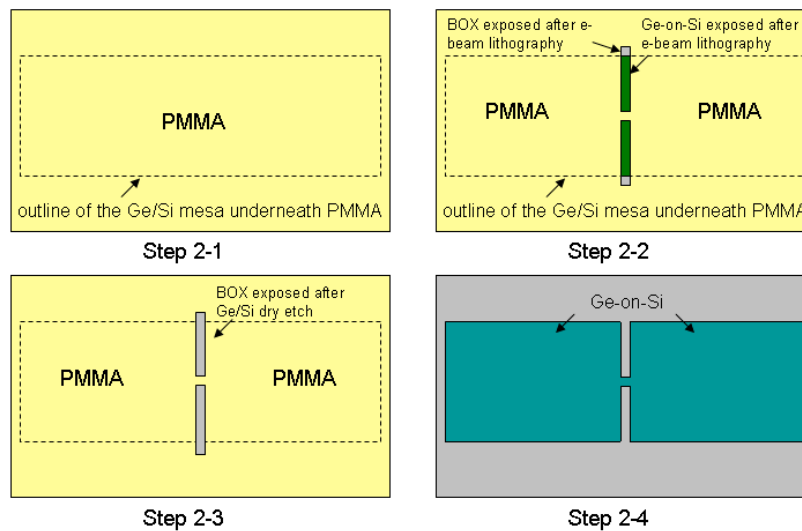


Fig. 3-7 Top view of STEP 2 in making nano-gate Photo-Hetero-JFETs

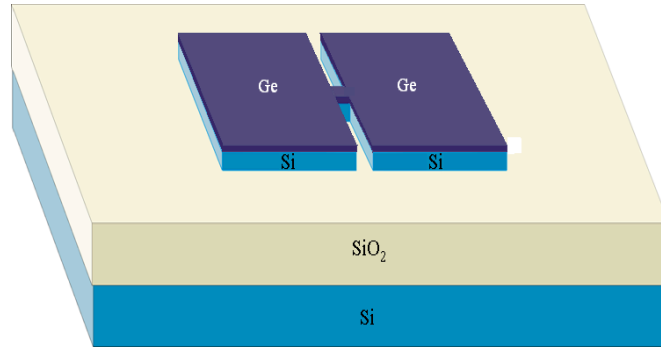
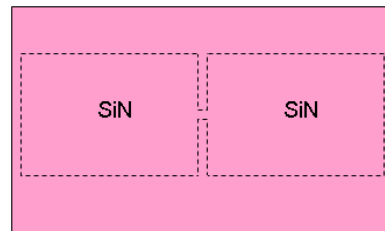


Fig. 3-8 Device structure after STEP 2

3.3.3 STEP 3

Next step is to pattern the nano gate which is 100nm in length. Since the source and drain are to be self-aligned to the gate, an ion implantation mask needs to cover the p-Ge gate and protect it from the n dopant ions. Therefore a silicon nitride layer of 200nm is first deposited everywhere on the die by Plasma-Enhanced Chemical Vapor Deposition. The reactant gases are NH_3 and 10% SiH_4 in Ar, and the substrate temperature is 350°C [89]. Since PECVD growth is isotropic, the sidewalls of the mesa that get exposed after the bridge is defined are then covered by the nitride. This protects the silicon channel sidewalls from implanted ions, and that's one main reason that the PECVD nitride layer is deposited after the bridge is formed.



Step 3

Fig. 3-9 Top view of STEP 3 in making nano-gate Photo-Hetero-JFETs

3.3.4 STEP 4

The second e-beam lithography is performed to pattern the gate of 100nm length. The same set of alignment marks is used. To leave margins for misalignment, the ebeam mask is written such that the size of gate feature is 100nm×1.4μm. Therefore, the first dimension 100nm determines the real channel length while the width of the bridge determines the real channel width, which is 1μm. A negative ebeam resist is used because the gate feature is what should remain after resist exposure and development. The resist chosen is MaN2403 from Microchem and it is ~300nm thick when spun at 3000rpm.

Dosetests on the resist writing the gate feature on the same substrate (PECVD nitride

layer) were carried out prior to the actual writing on the device die. After developing and DI water rinse, we found out that most of the $100\text{nm} \times 1.4\mu\text{m}$ bars are not where they were supposed to be. Some collapsed and others were simply gone. Although the aspect ratio of the resist bars does not sound high, most of them cannot survive structural collapse or do not stick well to the substrate. To solve this problem, two large squares ($\sim 500\text{nm} \times 500\text{nm}$ or $\sim 1\mu\text{m} \times 1\mu\text{m}$) are drawn on both ends of bar features (see Fig.3-10(a)), in order that the two big squares of resist adhere better to the substrate and then hold the bar in between that they are attached to. And as the separation between the source island and drain island is $1\mu\text{m}$ or $2\mu\text{m}$, squares of 500nm or $1\mu\text{m}$ will simply be drawn in the separation slot, respectively, even considering the possible alignment errors. In Fig.3-10 (a) and (b), attached to the $1\mu\text{m} \times 1\mu\text{m}$ squares on both ends, the 80nm resist bar stands and sticks very well to the substrate. The resist bar of this size would have collapsed or moved otherwise.

However, we found out later, on real device die, as the resist bar sitting on the bridge is longer than the bridge width, both ends of the resist bar simply lean on the side walls (see Fig.3-11 on an SOI dummy with bridge patterned out of its top silicon layer), which helps resist adhesion to the bridge. So the problem is actually self-solved owing to the nature of the previous device pattern. The SEM picture of the patterned resist with 100nm gate feature on the bridge is shown in Fig. 3-12.

The Silicon nitride layer of 200nm and the germanium layer of 110nm are then removed everywhere except under the negative ebeam resist by reactive ion etching. The nitride etcher has four symmetric electromagnetic coils located around the perimeter of the etch chamber [89]. With current flowing through the coils, a rotating magnetic field is produced, which causes more collisions between the free electrons and the gas molecules, resulting in a more ionized and reactive gas and therefore enhancing the etch process. The gas mixture that is used for silicon nitride etch in this etcher is CF_4/CHF_3 . With CHF_3 added to CF_4 , C to F ratio is increased resulting in more polymer inhibitor deposition to increase etch anisotropy or create more vertical sidewalls. Adding O_2 to the gas mixture helps to prevent too much inhibitor formation as O_2 reacts with the carbon. Small amount of O_2 also aids to increase the etch selectivity over the resist. The germanium film is etched in the same way as described in step 2. Finally MaN2403 is removed in heated acetone and mild sonication aids to the complete removal of the resist.

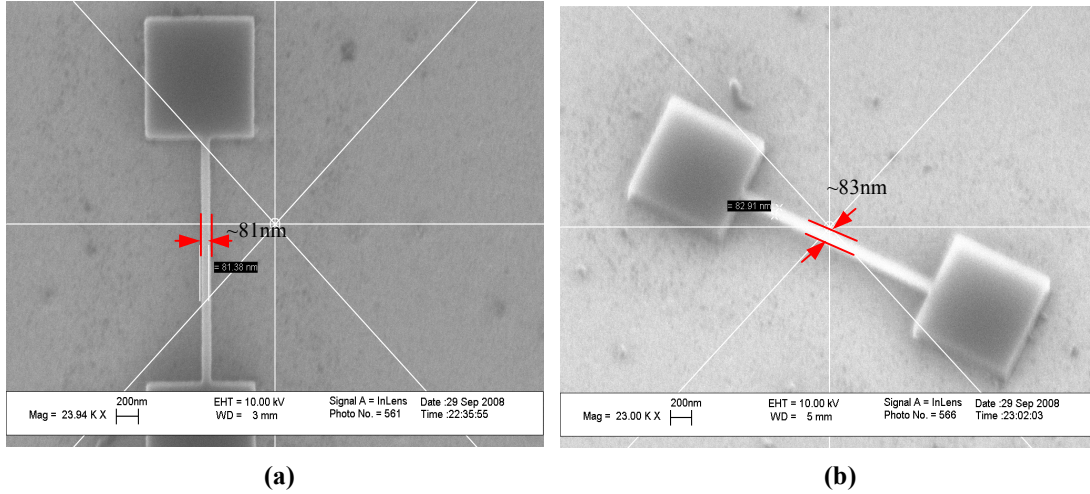


Fig. 3-10 SEM pictures of MaN resist after exposure and developing in (a) Top and (b) angled views. Two squares are attached to the 80nm bar so that the thin bar structure does not collapse.

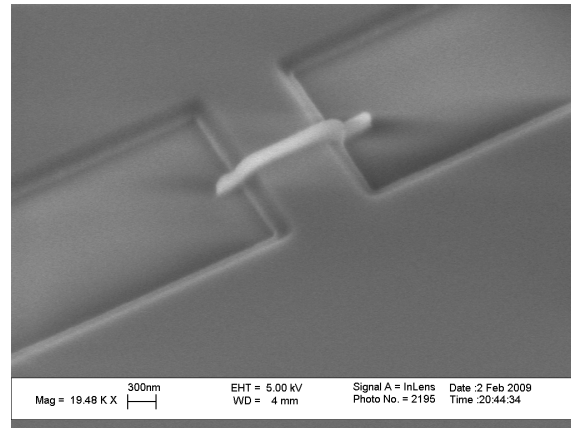


Fig. 3-11 SEM picture of a thin MaN resist bar (~100nm) sitting on Si bridge on an SOI dummy

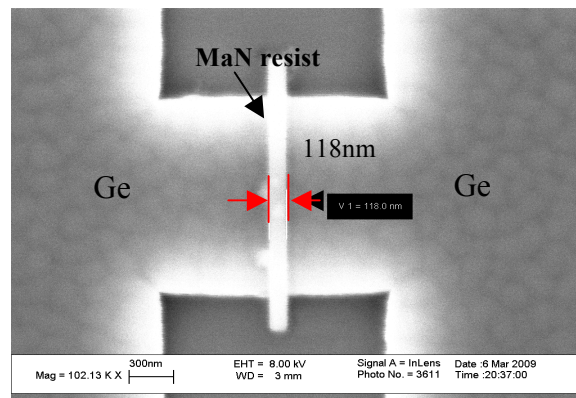


Fig. 3-12 SEM picture of an unfinished Photo-Hetero-JFET device in STEP 4. The MaN resist of the nano gate feature indeed sticks to germanium over the bridge.

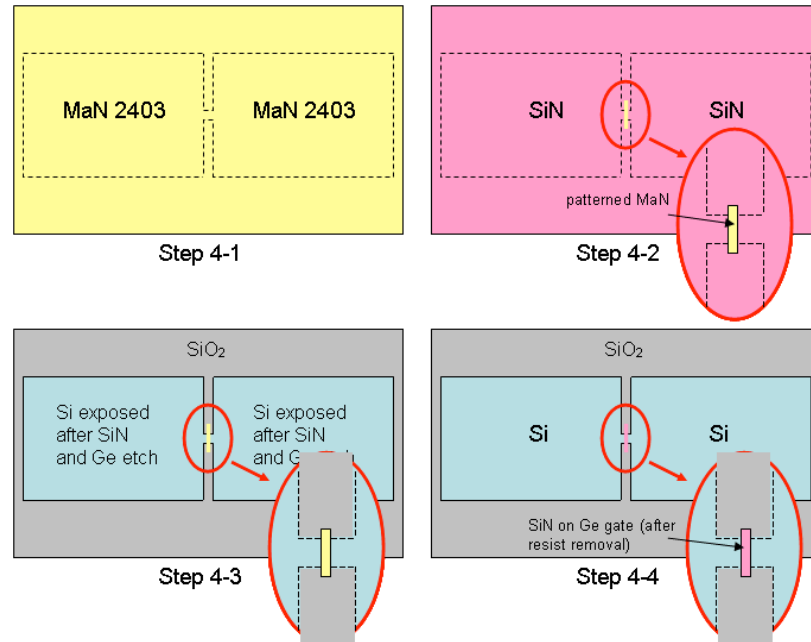


Fig.3-13 Top view of STEP 4 in making nano-gate Photo-Hetero-JFETs

3.3.5 STEP 5

A layer of ~10nm PECVD silicon oxide is grown on the sample prior to ion implantation. This oxide layer is there to randomize the implanted ions and prevent ion channeling in the crystalline silicon. Another way to prevent ion channeling is to tilt the wafer by 7° from its normal incidence orientation. However, since we do not want ions to go under the gate too much to dope the channel too far into n-type, we decide to keep the normal incidence orientation. Furthermore, the ion implantation chamber is usually contaminated with impurity ions, hence the need for this thin oxide serving as a protective layer.

3.3.6 STEP 6

The die is then sent out for ion implantation to create a heavily doped self-aligned source and drain region. There are many considerations that are involved in this step and the following annealing step.

I. Solid Phase Epitaxy

Typically the highly doped regions would be fabricated using high dose ion implantation followed by a high temperature anneal to repair the damage and activate the dopants. The annealing temperature, or the localized annealing by laser spikes, is normally in excess of 1000°C [77], which is well above the melting point of Germanium (940°C). Moreover, the intermixing between the Ge and Si is expected to be very pronounced in that temperature range. To avoid these problems, ideally Ge film should be grown after the

annealing. However, the implant and the subsequent high temperature processing can cause impurity segregation which would adversely affect the quality of Ge film grown. So this process flow that creates highly doped source and drain pockets on the silicon wafer that already has Ge layer on it, is preferred. The requirement for this process flow is such that the temperature during the fabrication should not approach 940°C and in fact should be kept as low as possible to avoid the inter-diffusion of Ge and Si [77].

Solid Phase Epitaxy (SPE) [91, 92] is thus introduced in this fabrication process to achieve this goal. In this technique, the initial implantation of Si with the desired dopant species is carried out with *extremely high dosage* so that the damage is high enough to completely amorphize the substrate, while *the energy of the implant is kept low* enough so as to restrict the amorphization to the superficial layers in the silicon, leaving the silicon underneath the damaged layer intact as single crystalline. This single crystalline silicon then acts as a seed layer for the amorphous top layer to recrystallize itself even at moderate temperatures, thereby fixing the damage in the top silicon and activating the dopants. This process of restoring its crystalline phase is referred to as Solid Phase Epitaxial Regrowth (SPER). The temperatures required for SPE are in the range of 500 to 700°C which is well below the thermal budget established for germanium-on-silicon system and thus makes it extremely useful. One problem with this technique that requires notice is that, end-of-range (EOR) defects [91] can exist at the original interface of amorphous and single crystal layers due to incomplete amorphization in that region, the complete removal of which requires temperature still above 1000°C. Those defects can increase the leakage current seen in transistors fabricated from the recrystallized substrates. Such an adverse effect is often reduced by excluding EOR defects out of depletion region.

In conclusion, the technique of SPE is applied here to implant and anneal the silicon to create source and drain regions for Photo-Hetero-JFETs. Low implant energy and a high ion dosage are required, which would result in source and drain region kept quite close to the surface.

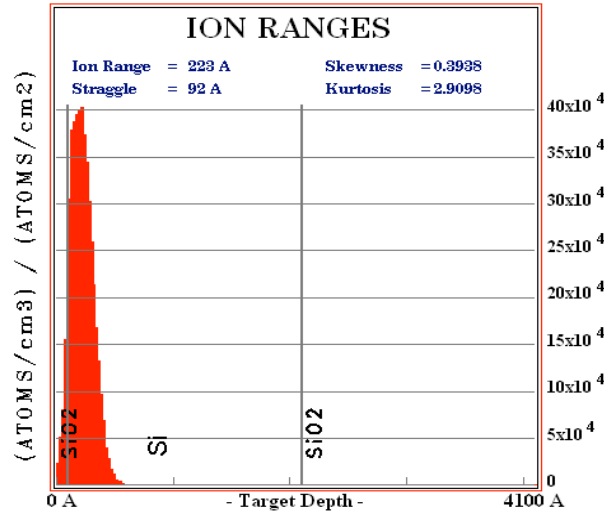
II. Process Parameters Design for Ion Implantation and Annealing

Recall that we also want to dope the silicon underneath the gate with this ion implantation step for the favored junction band structure, and the desired silicon channel doping concentration to be achieved after the post-implant annealing is $2.5 \times 10^{16} \text{cm}^{-3}$. Therefore, careful design and process simulation has to be done in order to choose the right parameters for both the implant and annealing process.

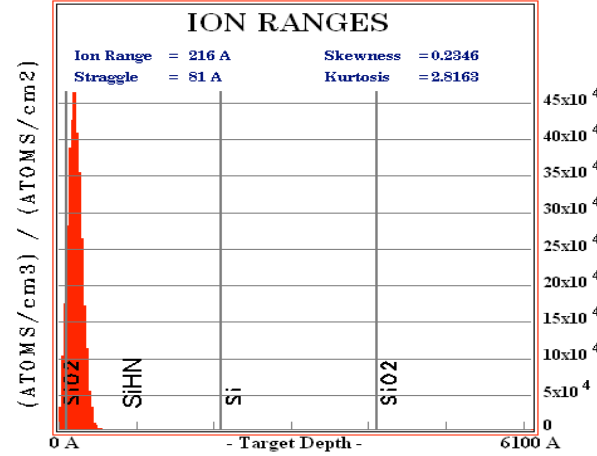
As lateral straggle range increases with the projected ion range, with mask only ~100nm wide, ion implant energy again should be kept low to avoid too much lateral straggle that indirectly dope the channel too far in n-type. Phosphorus is chosen as the n-type dopant

species, for it is lighter than arsenic and thus produces relatively less damage. The ion energy chosen is 12keV and the dosage is $1.2 \times 10^{15} \text{ cm}^{-2}$.

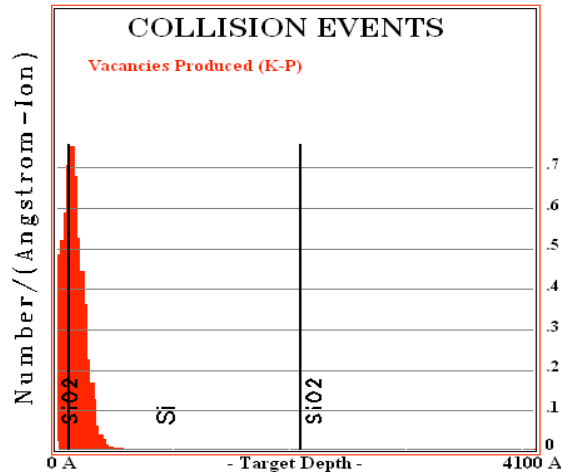
With this, the projected ranges of phosphorus into the oxide covered Si and the nitride mask on the gate are predicted through simulation of particle interaction with matter by standard SRIM (the **S**topping and **R**ange of **I**ons in **M**atter) software, shown in Fig.3-14 (a) and (b). Since the silicon nitride is deposited using a low temperature PECVD process, it is expected to have significant H contamination which can in turn lower its density [89]. The target in the plot for phosphorus implantation into nitride was therefore assumed to be SiNH (with a density of 2.2 g/cc) instead of Si_3N_4 . As indicated in Fig. 3-14(b) the maximum penetration depth of P^{31} in SiNH is found to be $< 50\text{nm}$, therefore the 200nm nitride mask is clearly thick enough to ensure that none of the dopant atoms enter the Ge. Fig. 3-14(c) shows that the peak density of vacancies produced in the silicon is $\sim 0.75/(\text{Incident Ion}) \cdot (\text{\AA})$. Therefore for a dose of $1.2 \times 10^{15} \text{ cm}^{-2}$, the density of vacancies would be $\sim 9 \times 10^{22} \text{ cm}^{-3}$, which far exceeds the amorphization threshold in the Silicon. Also from Fig. 3-14(a) it is seen that the range of P^{31} ions in the Silicon is $\sim 30\text{nm}$, which means that the amorphization is indeed restricted to the superficial layers in the substrate, and hence we have good single crystal seed layer for the amorphized top layer to restore crystalline in the annealing step that followed. The lateral straggle range predicted by SRIM in the silicon is $\sim 10\text{nm}$, which will be extended further by ion diffusion during annealing.



(a)



(b)



(c)

Fig. 3-14 Expected implantation profiles for Phosphorus (12keV, no tilt) calculated using standard Stopping Range of Ions in Matter (SRIM) software. (a) Range of P^+ ions in Silicon (b) Range of P^+ ions in Silicon Nitride (c) Damage profile in Silicon in terms of number of vacancies produced.

While ion projected range, initial lateral straggle and damage in the silicon are estimated first in TRIM, the final doping profile including channel, source and drain in silicon can be found out by simulating the ion implantation and rapid thermal annealing (RTA) steps in FLOOPS (FLorida Objected Oriented Process Simulator) included in ISE package. The desired doping profile is achieved (shown in Fig.3-15) when the parameters for RTA are chosen such that the annealing temperature is 650°C and the annealing duration is 5mins. From Fig.3-15, we see that the active doping concentration in the source and drain regions are above $\sim 1 \times 10^{20} \text{ cm}^{-3}$ to the depth of 50nm, and the average doping concentration in the channel is $\sim 2.5 \times 10^{16} \text{ cm}^{-3}$, which should result in the silicon channel

completely depleted under the p-Ge gate. However, the dark current measured in a Photo-Hetero-JFET device indicates that the real average channel doping concentration is $3\sim 4\times 10^{16}\text{cm}^{-3}$, which is quite close to the simulated value.

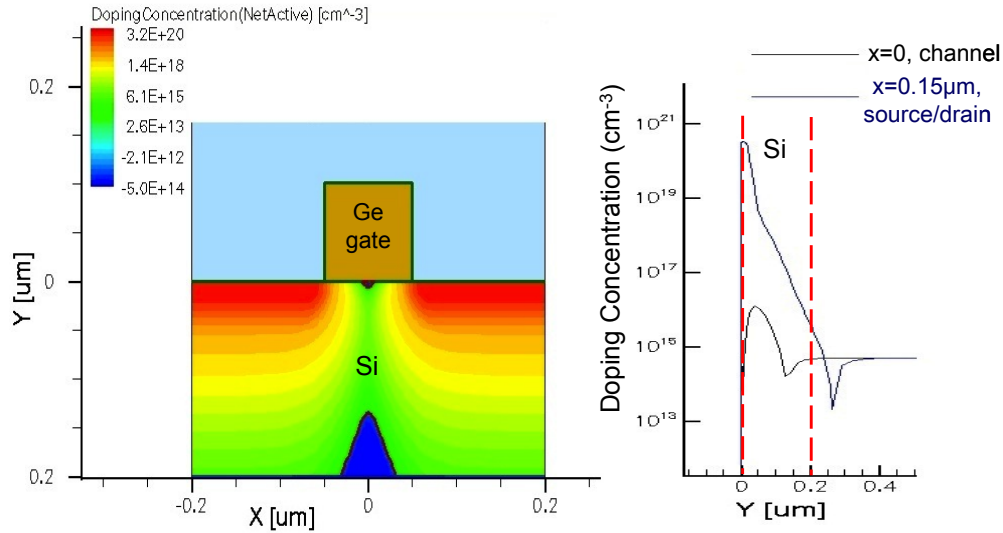


Fig.3-15 Simulated doping profile in silicon after masked ion implantation and RTA steps. It clearly shows the formation of heavily doped source and drain self-aligned to the 100nm long channel which is counter-doped to n-type, thanks to the lateral straggle in ion implantation step and ion diffusion in the subsequent RTA step. The simulation is done in FLOOPS.

So we followed our design and sent out the die after STEP 5 to CoreSystems for ion implantation. Phosphorus ions with 12keV energy and dose of $1.2\times 10^{15}\text{cm}^{-2}$ are implanted into the substrate held with 0° tilt.

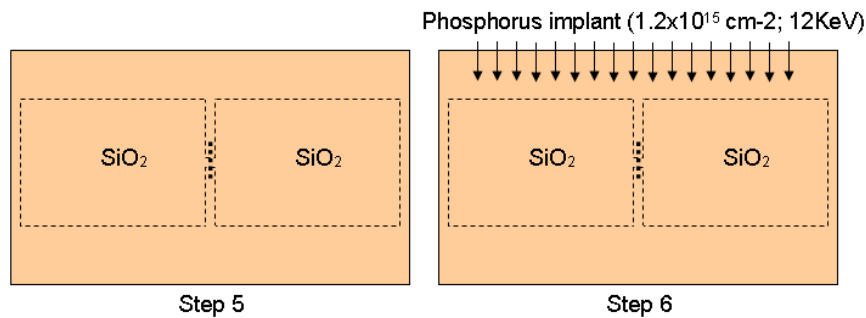


Fig.3-16 Top view of STEP 5 and STEP 6 in making nano-gate Photo-Hetero-JFETs

3.3.7 STEP 7

After the implanted dies are sent back, the protective oxide layer is first stripped off by dipping into diluted HF solution (49% HF 1:10).

The silicon nitride mask on the gate is then etched in a hot phosphorus acid bath at 160°C. The hot phosphorus acid is preferred over HF/BOE owing to its high etch selectivity of silicon nitride over silicon oxide, while in HF/BOE solutions, silicon oxide goes almost two orders of magnitude faster than silicon nitride. So if our JFET structure were immersed in HF/BOE solution, the buried oxide in the bridge would be gone long before the nitride mask layer.

Berkeley Microlab developed a system to control the temperature and concentration of the hot phosphorus acid bath to ensure controlled etch rate of silicon nitride [93]. They use a water injection system which is linked to the temperature of the bath to compensate the water content that get decreased due to evaporation. When the bath reaches set point, a signal is generated by the temperature controller that stops firing the bath heater. This same signal is tied to the DI water injection valve – the valve is opened for a defined amount of time to allow an injection of fresh DI water into the bath. The length of time that the injection valve is opened also determines the etch rate and has been optimized. The etch rate calibrated for the PECVD silicon nitride is roughly 40nm/min.

3.3.8 STEP 8

After removal of oxide protective layer and nitride mask layer, a 100 nm PECVD silicon oxide is deposited, which acts as a protective layer during the annealing.

3.3.9 STEP 9

The device sample is then loaded into a rapid thermal annealing unit, and annealed in nitrogen ambient at 650°C for 5 minutes. As mentioned previous in the introduction to SPE, even the relatively low-temperature anneal is expected to activate the dopants and cure most of the implant damage. Dummy SOI wafers that were subjected to the same ion implantation step were loaded together with the device sample and also went through the same RTA process. They are prepared for characterization of the contact resistance and the sheet resistance of the heavily doped regions.

The protective oxide layer is removed in diluted HF solution (10:1 49% HF) after RTA. The device structure after this is depicted in Fig. 3-17.

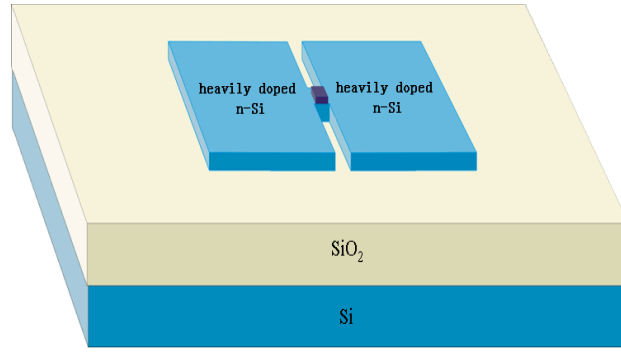


Fig. 3-17 Device structure after STEP 9

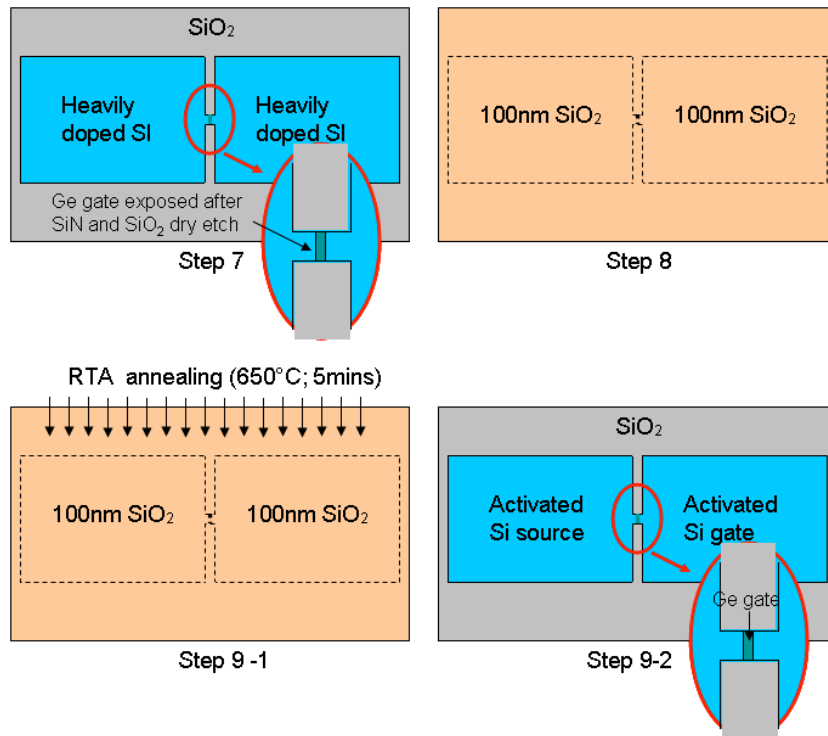


Fig. 3-18 Top view of STEP 7 through STEP 9 in making nano-gate Photo-Hetero-JFETs

3.3.10 STEP 10

Finally, the metal contacts (25\AA Ti/ 1500\AA Al/ 50\AA Ti/ 1000\AA Au) are deposited on the source and drain regions by standard photolithography and liftoff (See Fig. 3-20). Again, Ti is used for adhesion and Au is here to prevent Al from being oxidized and to aid wire-bonding.

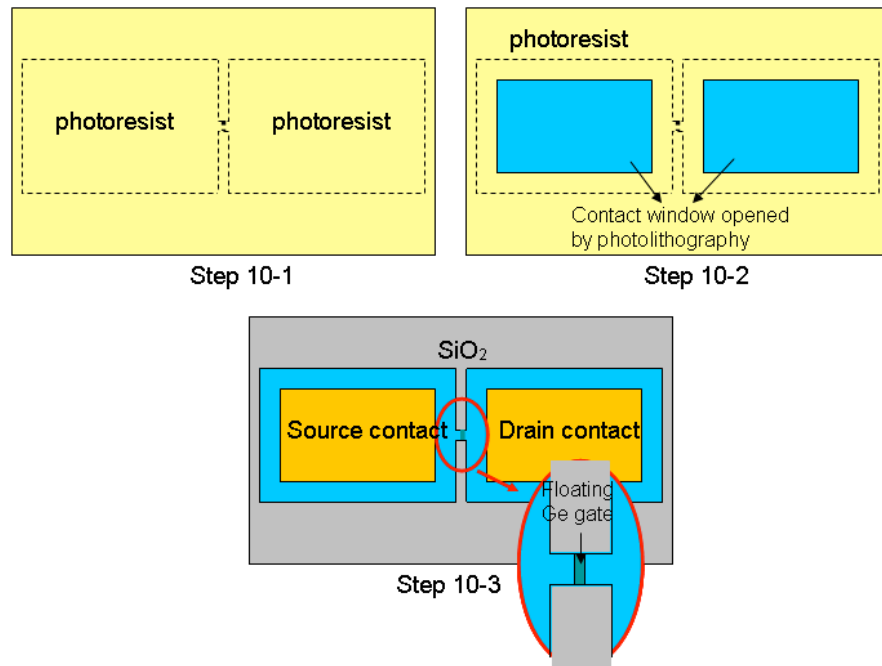


Fig. 3-19 Top view of STEP 10 in making nano-gate Photo-Hetero-JFETs

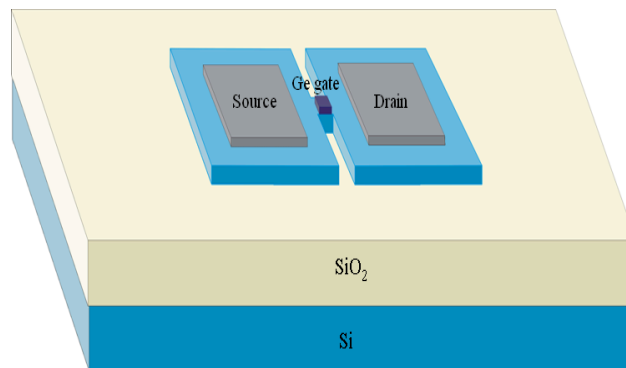


Fig. 3-20 Device structure after STEP 10

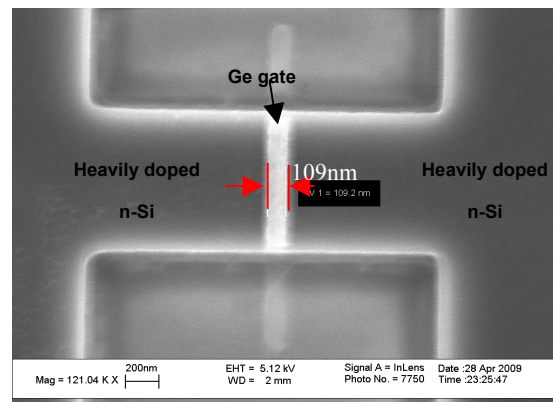


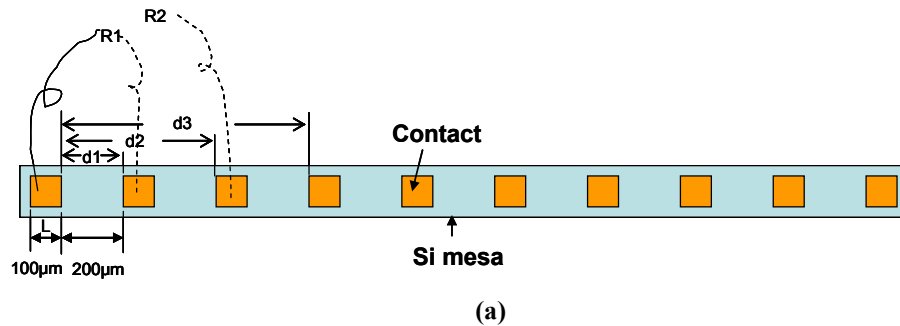
Fig. 3-21 SEM picture of a finished Photo-Hetero-JFET zoomed in around the germanium gate

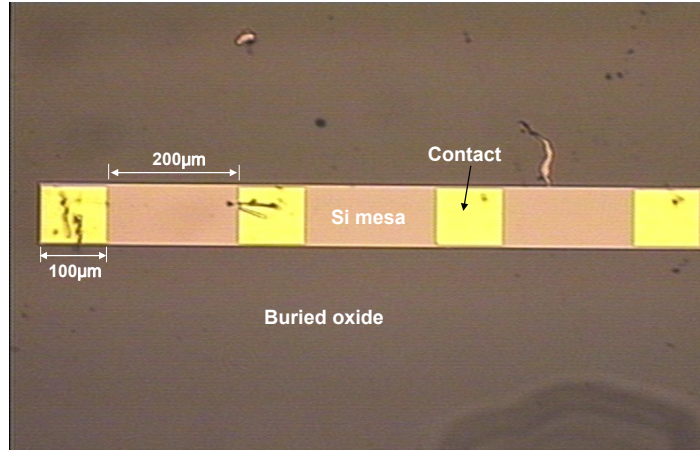
Fig.3-21 shows the SEM micrograph of one of the finished devices. The samples are finally cleaved and wire-bonded onto high speed chip carriers that have a micro-strip active contact pad. The wire bonds are kept as small as possible in order to minimize the parasitic inductance in the circuit.

At the same time, a line of $100\mu\text{m} \times 100\mu\text{m}$ squares of the same metal stacks separated by $200\mu\text{m}$ each are deposited on one dummy SOI sample (Fig. 3-22 (a) and (b)). Resistances between different pairs of contacts are to be probed to extract contact resistance and sheet resistance. This method of characterizing contact resistance is called *transfer length method (TLM)* [93]. To reduce the lateral current crowding, silicon mesa of width slightly larger than that of contacts is etched to reduce currents flowing around the contacts that introduce errors. The resistances are probed between the first contact pad and other contact pads. A plot of total resistance as a function of contact spacing is in Fig. 3-23.

Since the total resistance between any two contacts is $R_T = \frac{\rho_s d}{Z} + 2R_c$ [93], the fit of the plot indicates that the contact resistance is around $\sim 75\Omega$, and the sheet resistance is $\sim 7.4\Omega/\square$, which indicate that the doping level in the source and drain is $\sim 5.9 \times 10^{20}/\text{cm}^3$, which is expected from the dosage level used during the implant.

One may notice that the total resistance data does not fit to a linear plot. The reason for this deviation is that when probing the two contacts except for the first two, the current flow may be perturbed by the contacts between them [93]. If the contact length L is much bigger than the so-called transfer length L_T , the current does flow into the metal of the contacts in between. This shunting of the current by the contact metal strip(s) obviously influences the total resistance probed. Therefore, the real contact resistance should be even smaller than $\sim 75\Omega$, indicating good formation of the source and drain contacts in Photo-Hetero-JFETs. A preferred test structure of TLM is in fact with unequal spacing between contacts as in Fig. 3-24, with the resistance measured between adjacent contacts.





(b)

Fig.3-22 Lines of contacts deposited on silicon mesa for TLM. (a) schematic of test structure and probing method (b) microscope picture of test sample

Finally, the samples are cleaved and wire-bonded onto high speed chip carriers that have a micro-strip active contact pad. The wire bonds are kept as small as possible in order to minimize the parasitic inductance in the circuit. This concludes the fabrication of the nano-gate Photo-Hetero-JFETs.

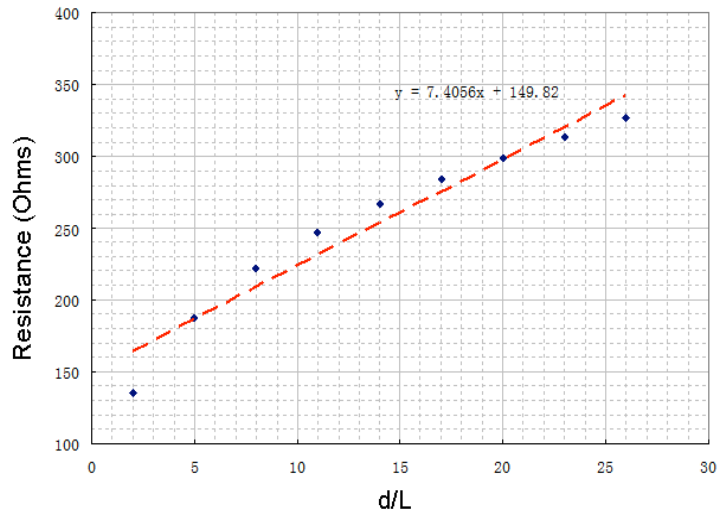


Fig. 3-23 Total resistance probed on pairs of contacts versus contact spacing

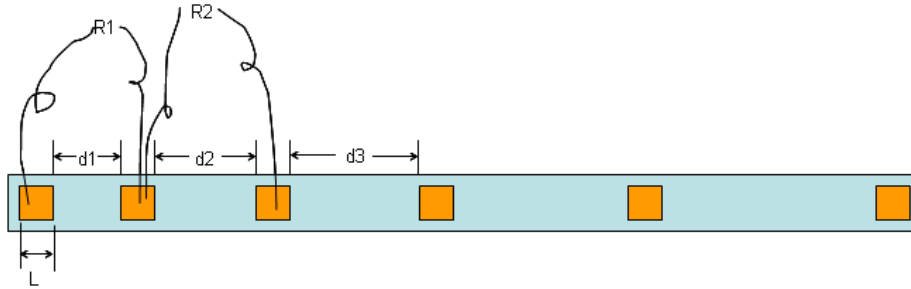


Fig. 3-24 Preferred test structure of TLM with unequal contact spacing

Both heterojunction diode devices and Photo-Hetero-JFET devices were fabricated in the cleanroom facilities of the Microlab at Berkeley. The fabrication process of Photo-Hetero-JFET devices uses ebeam lithography for 100nm gate feature definition, as it is faster, easier and less costly for making prototyped devices than photolithography. But Photo-Hetero-JFETs with 100nm or even shorter channel lengths can be easily made using state-of-the-art photolithography techniques in industry. Actually from the process flow described above, we see that the fabrication process of Photo-Hetero-JFETs is all CMOS compatible, and the device can easily be scaled down without altering this CMOS-compatible process.

Chapter 4 Device Characterization and Analysis

The main task of this chapter is to describe the experimental characterization of the Photo-Hetero-JFET and to analyze its photoresponse in proper physical models. Since the Photo-Hetero-JFET is a transistor that is built under a p-Ge/Si heterojunction in which photodetection actually happens, the heterojunction diode device is also characterized to provide basis for the understanding of the transistor device (throughout this chapter, the transistor device refers to the Photo-Hetero-JFET, and the diode device refers to the p-Ge/Si heterojunction diode).

4.1 Characterization of heterojunction diode device

As said in Chapter 2, in Photo-Hetero-JFETs, p-Ge gate/Si channel junction is where all the interesting physics of the detector happens. Therefore, characterization of this heterojunction diode is very important in understanding and characterizing the performance of the transistor device.

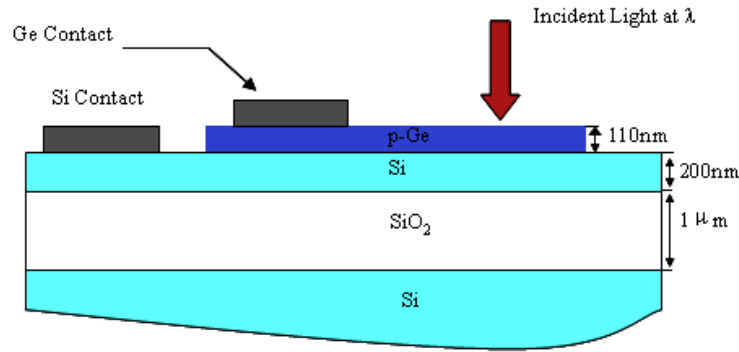


Fig.4-1 Cross-section view of the heterojunction diode device

4.1.1 Responsivity measurements of the heterojunction diode

The responsivity measurements are performed on the heterojunction diode devices shown in Fig.4-1. Continuous-wave near-infrared light at both 1.3μm and 1.55μm are focused and normally incident on the p-germanium mesa. The p-Ge side and Si side are connected through a resistor to a variable voltage source with an ammeter in series.

4.1.2 Junction I-V curves

The I-V curves of the diode with and without light are probed and shown in Fig.4-2 (a) and (b). We can see that the forward current is clearly saturated by series resistance. This is expected since the p-Si layer is highly resistive, so the plots need to be corrected for series resistance in order to be accurate. Fig.4-3 (a) and (b) show the I-V curves with actual voltage that drops across the p-Ge/Si junction on the x-axis. The corrected voltage

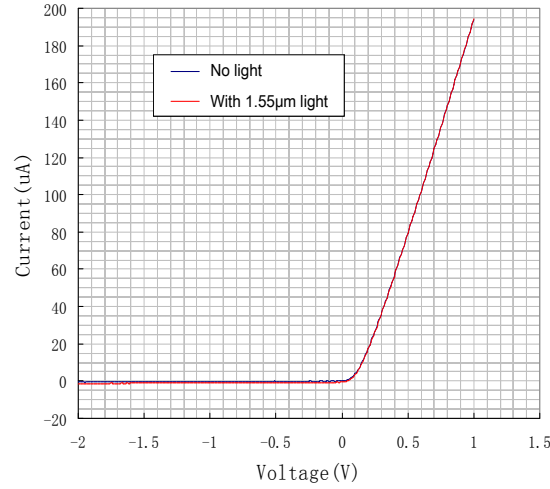
at each data point is obtained by subtracting the voltage drop across the series resistance, which is estimated from the slope of the original I-V curve in forward direction. A zoomed-in plot at small voltage biases with all three I-V curves (no light, with 1.55 μm light, and with 1.3 μm light) is presented in Fig.4-4. Fitting the IV curves to a diode equation is crucial for analyzing the subsequent devices because it gives us an excellent tool to parameterize the p-Ge/Si junction. The following expression accurately fits the *dark* plots (the fit is plotted in Fig.4-4 too):

$$I = 2.25 \times 10^{-7} (e^{\frac{qV}{1.14kT}} - 1) \text{ Amps.}$$

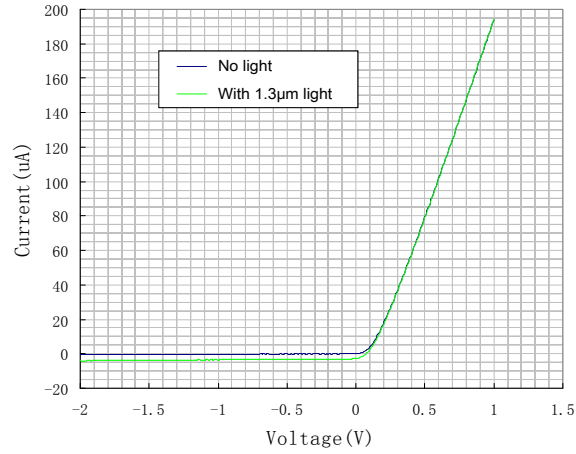
The dark current is hence 0.225 μA , and the qualify factor is 1.14. Considering the cross-section of the p-Ge/Si junction is 400 μm ×400 μm , the normalized diode equation describing the current density is then:

$$J = 1.41 \times 10^{-4} (e^{\frac{qV}{1.14kT}} - 1) \text{ Amps/cm}^2.$$

It is worth emphasizing again that this diode equation and these extracted parameters are important in understanding the mechanism and performance of the Photo-Hetero-JFETs, which will be further discussed later in this chapter.

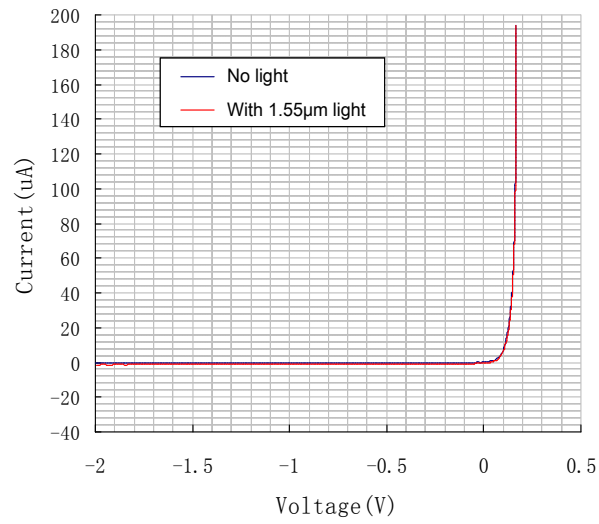


(a)

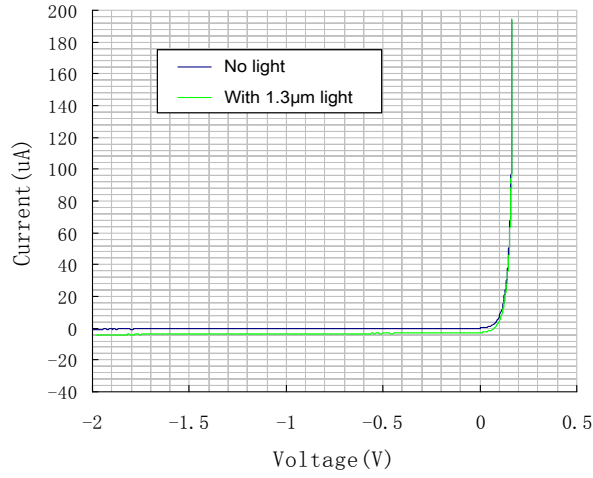


(b)

Fig. 4-2 I-V curves with and without light for 400 μ m x 400 μ m p-Ge mesas on n-SOI: (a) 1.55 μ m light, 3mW (b) 1.55 μ m light, 2.5mW.



(a)



(b)

Fig.4-3 I-V curves with and without light for 400μm x 400μm p-Ge mesas on n-SOI, corrected for series resistance: (a) 1.55μm light, 3mW (b) 1.55μm light, 2.5mW.

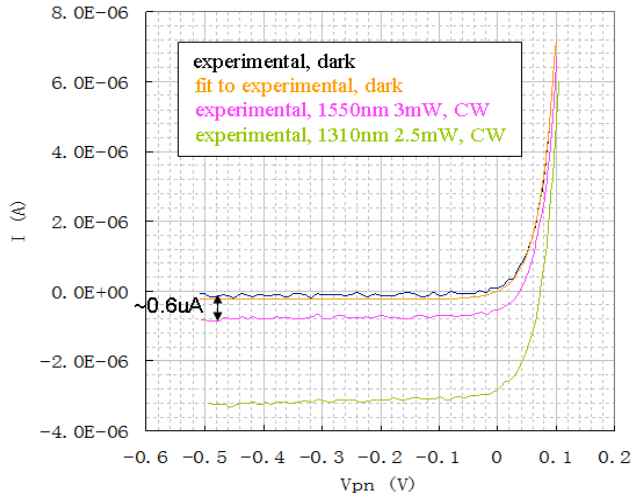


Fig.4-4 A zoomed-in plot of all three I-V curves (dark, with 1.55μm light, and with 1.3μm light). Numerical fit to the dark I-V curve is also shown.

4.1.3 Responsivity and diffusion length

The photocurrents in the hetero-junction diode under zero bias at both wavelengths can be learned from the I-V curves in Fig.4-4:

$$I_{1ph} = 0.6\mu A$$

for 3mW illumination at 1550nm and

$$I_{2ph} = 2.8\mu A$$

for 2.5mW illumination at 1310nm. So the responsivity of hetero-junction diode under zero bias at both wavelengths are

$$R_1 = 2e - 4 A/W \quad \text{for 1550nm,}$$

$$R_2 = 1.12e - 3 A/W \quad \text{for 1310nm.}$$

The quantum efficiency values at these two wavelengths are therefore

$$\eta_1 = \frac{hv}{q} R_1 = 0.8 \times 2e - 4 = 1.6e - 4,$$

$$\eta_2 = \frac{hv}{q} R_2 = 0.946 \times 1.12e - 3 = 1.06e - 3,$$

which are not very promising.

We first assume that the diffusion length model is applicable to explain the relatively poor quantum efficiency. From our earlier discussion in Chapter 2, it is shown that diffusion length can be extracted from responsivity as

$$L_D = \frac{hv}{q} \cdot \frac{R}{(1-r)\alpha} = \frac{\eta}{(1-r)\alpha} \quad (4.1),$$

if everything else on the left-hand side of the equation is also known. The reflectivity of air/germanium interface r is 0.4. The values of absorption coefficient α for germanium at both wavelengths can be referred in Fig.4-5. For single-crystalline germanium, as the wavelength of 1550nm gets very close to its absorption edge, the α value at 1550nm is not very well-defined. Although in poly-crystalline germanium, the absorption spectrum seems to be extended and the value of absorption coefficient is raised at wavelengths beyond 1500nm, possibly due to the increase of defect-induced electronic states within the bandgap, the absorption coefficient value at 1550nm is still considered less reliable than that at 1310nm, which is $14,000\text{cm}^{-1}$. Thus it's more accurate to extract the "diffusion length" from the responsivity at 1310nm. Again, our previous point that the diffusion length L_D , independent of wavelength of illumination, is more an inherent property than is responsivity in characterizing germanium film. The "diffusion length" is estimated from the responsivity at 1310nm to be

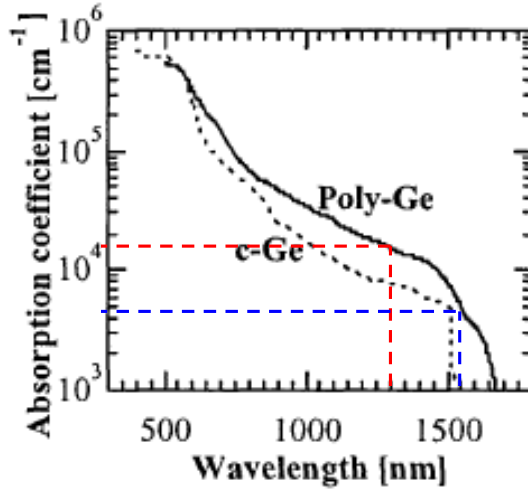


Fig.4-5 absorption spectrum of c-Ge and Poly-Ge, reproduced from ref. [13].

$$L_D = \frac{\eta_{1310nm}}{(1-r)\alpha_{1310nm}} = \frac{1.06e-3}{(1-0.4) \times 14,000cm} = 1.26nm.$$

From this extracted value of diffusion length, which is wavelength-independent, together with photoresponsivity at 1550nm, one can further estimate the absorption coefficient at 1550nm to be

$$\alpha_{1550nm} = \frac{\eta_{1550nm}}{(1-r)L_D} = \frac{1.6e-4}{(1-0.4) \times 1.26e-7cm} = 2113.2cm^{-1},$$

This is about half of the suggested value in Fig.4-5. Moreover, one can calculate the “internal quantum efficiency” of the germanium mesa in the junction based on the estimated diffusion length. “Internal” quantum efficiency, in the context of solar cell, refers to the efficiency with which photons that are not reflected or transmitted out of the cell can generate collectable carriers. Here, in this p-Ge/Si heterojunction device, the internal quantum efficiency is hence the percentage of photocarriers absorbed within diffusion length to that absorbed in the entire germanium film, i.e. the ratio of the effective electron diffusion length to the germanium mesa thickness,

$$\eta_{int} = \frac{L_D}{L_{Ge}} = 1.26\%.$$

This internal quantum efficiency value, decoupled from other factors including light coupling and absorption efficiencies, also serves as an indication of germanium material quality.

4.1.4 Estimate of the worst diffusion length

The diffusion length estimated from the poor quantum efficiency of p-Ge/Si heterojunction diode appears to be unreasonably small. In order to prove or disprove the validity of the diffusion length model in its applicability to this poly-Ge/Si diode, the worst possible diffusion length in a semiconductor is estimated as below.

Assume that a piece of semiconductor is of worst possible quality. It is very defective with extremely large density of traps. The trap concentration is so large that we assume they are closely spaced and their capture cross-sections just correspond to the spacings. Therefore [95],

$$\tau_r = \frac{1}{N_t \cdot v_{th} \cdot \sigma} = \frac{1}{\frac{1}{\sigma^{3/2}} \cdot v_{th} \cdot \sigma} = \frac{\sigma^{1/2}}{v_{th}}.$$

in which the thermal velocity v_{th} is 10^7 cm/sec. A reasonable value for capture cross-section σ in the semiconductor is 10^{-15} cm² (roughly $3\text{\AA} \times 3\text{\AA}$). Therefore the free carrier lifetime τ_r in this extreme case is calculated to be 3×10^{-15} s.

Carrier mobility in a semiconductor can be estimated from its mean free path l_p because

$$\mu = \frac{q\tau_m}{m} = \frac{ql_p}{mv_{th}}.$$

In the worst case scenario, mean free path l_p can be as small as 5\AA , the cubic crystal unit cell length. This gives the worst mobility in a semiconductor to be $\mu = 90 \text{ cm}^2/\text{V}\cdot\text{s}$. Combining these two worst-case values (τ_r and μ), a worst-case diffusion length L_D is hence

$$L_D = \sqrt{D \cdot \tau_r} = \sqrt{\frac{kT}{q} \mu \cdot \tau_r} = \sqrt{0.025 \times 90 \times 3 \times 10^{-15}} = 8.2 \times 10^{-8} \text{ cm} = 0.82 \text{\AA}.$$

A diffusion length of this extremely small value suggests that physically the carriers simply recombine where they are generated – there's not really any diffusion. Since the diffusion length that we extracted from the responsivity is almost as small as this extreme-case diffusion length value. It is believed that the diffusion length model may not be appropriate in explaining the poor quantum efficiency of the pGe/Si diode.

4.1.5 Geminate recombination

A more realistic explanation to explain the poor quantum efficiency is *geminate recombination* [79, 80]. As introduced in Chapter 2, geminate recombination refers to the phenomenon that a photo-generated electron-hole pair recombines with its parent partner before any obvious diffusion occurs. In disordered semiconductor materials used in solar

cells and in photodetectors, a large number of photocarriers are lost in this manner at the very early stage. The rest of the photo-generated carriers that survived geminate recombination, can then separate away from their parent partners, travel the distance of a diffusion length on average, and recombine with the partners who are not necessarily from the same parent excitons as themselves. For the pGe/Si photodiode, what most likely happens to the photo-carriers generated in germanium is that, *firstly the majority of photocarriers generated are lost due to geminate recombination, and then among the rest, in an average sense, all that are generated outside the real diffusion length from the pGe/Si interface fail to survive the normal recombination.* Note that the real diffusion length in this so-called “polycrystalline” germanium could be on the same order of the worst-case value ($\sim 0.8\text{nm}$). That’s why only 0.02% of the photocarriers generated in the case of 1550nm laser illumination are finally collected as useful current.

On the other hand, the fact that we resort to geminate recombination in the interpretation of quantum efficiency also reveals that the quality of germanium thermally evaporated on SOI could be much worse than simply being “polycrystalline”. Owing to the reason mentioned earlier in Chapter 2, the growth temperature of germanium film on SOI substrate is less well-controlled and could be much lower than that required for the growth of poly-crystalline films. The evaporated germanium on SOI can be amorphous and thus geminate recombination is very likely present.

Nonetheless, the responsivity measurements done on the hetero p-Ge/Si photodiodes and the quantum efficiency analysis followed are useful information of possible photocurrent “seed” from which the Photo-Hetero-JFETs “amplify” from. In other words, such information provides grounds in either the transistor model or the photoconductor model in which the photodetector gain is to be analyzed.

Time-resolved photoresponse measurements are also done on the hetero pGe/Si photodiodes under zero bias. However, in the organization of this chapter, it will be discussed after the characterization of Photo-Hetero-JFETs, for the reason that time-resolved photoresponse measurements on the photodiodes were actually done after the characterization of transistor devices and were only intended for understanding the transient photoresponse of the transistor devices.

4.2 Characterization of Photo-Hetero-JFET devices

4.2.1 Continuous-wave photoresponse

The Photo-Hetero-JFET devices are first characterized with a continuous-wave laser at 1550nm. The measurement set-up is shown in the schematics drawn below (Fig.4-6).

The optical set-up for focusing and aligning the laser with respect to the device-under-test is standard. The 1550nm laser light from the fiber is collimated into free space and then divided by a non-polarized beamsplitter into two beams. One beam is directed into a high NA objective and focused onto the device. The reflected beam from the device sample goes back into the objective and part of it is redirected by the beamsplitter into a CCD camera. The image of the laser spot and the device under the illumination of the scattered light are hence displayed on the monitor connected to the CCD camera. By adjusting the micropositioner that controls the objective together with the beam-splitter and the collimating lens, the laser spot is aligned to the submicron germanium gate of the JFET. Adjustment of focus is also monitored through the display of the camera. Note that the focused laser spot A_{spot} is $\sim 50\mu\text{m}^2$, but the germanium gate A_{gate} is only $\sim 100\text{nm} \times 1\mu\text{m}$ in size. So in analysis of the external quantum efficiency, a factor of $A_{\text{gate}}/A_{\text{spot}}$ should be added.

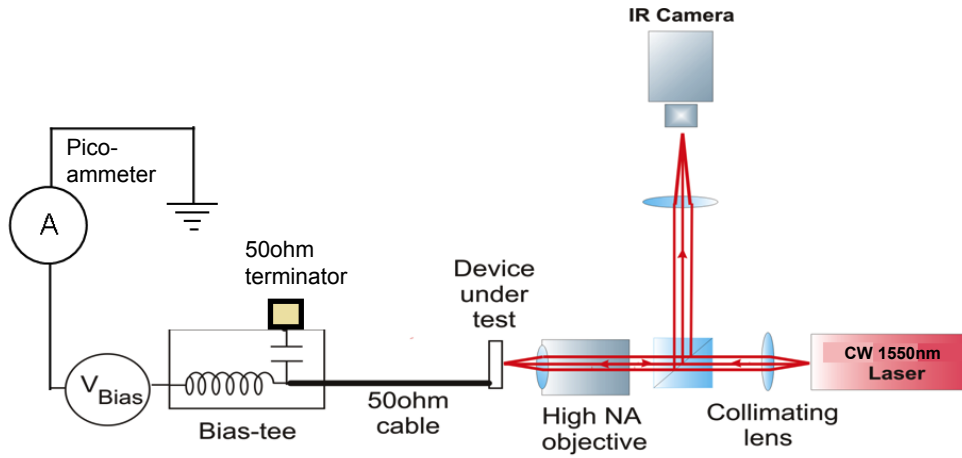


Fig.4-6 Schematic of the experimental set-up of continuous wave measurement on the Photo-Hetero-JFET.

The Photo-Hetero-JFET device, also referred to as the transistor device throughout the thesis, has been bonded to a high-speed chip carrier for the time-resolved transient characterization. The source contact is bonded onto ground pad of the chip carrier while the drain contact is bonded on the signal pad. So with the Photo-Hetero-JFET device mounted in this way, even in characterizing the DC response of the transistor device, the DC drain-to-source bias is still applied through the inductive arm of a bias-tee, and the capacitive arm of the bias-tee is terminated by a 50Ω terminator. For the same reason, a 50Ω cable is used here to connect the chip carrier through a SMA connector to the bias-tee. In the bias/measurement circuit, a picoammeter is connected in series with the device and the drain-to-source bias to monitor the change in channel current under the light. The drain-to-source bias is set at $V_{\text{DS}} = 0.5\text{V}$. Please refer to the circuit diagram in Fig.4-7 for clarification.

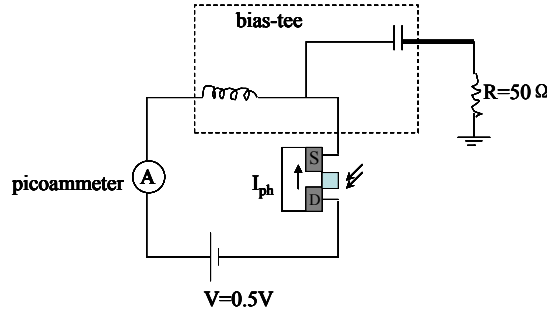


Fig.4-7 circuit diagram of the CW characterization of the Photo-Hetero-JFET

The dark current in the Photo-Hetero-JFET under a drain-to-source bias of 0.5V is 35.63 μ A, which indicates an initial channel resistance of 14k Ω . This is therefore suggestive of an average channel doping of $3 \times 10^{16} \text{cm}^{-3}$. The actual doping in the channel is a bit higher than the targeted doping level of $2.5 \times 10^{16} \text{cm}^{-3}$ for a completely depleted channel. As mentioned in Chapter 3, the counter-doping of silicon channel is achieved through ion lateral straggle in the self-aligned ion implantation and ion diffusion during the post-implant annealing processes. When the 3mW 1550nm laser is incident on the germanium gate of the Photo-Hetero-JFET, the increase in the channel current is 0.9 μ A. This corresponds to a CW responsivity of

$$R = 3 \times 10^{-4} \text{ A/W}$$

for the Photo-Hetero-JFET. According to the previously measured responsivity of the heterojunction diode device, in a hetero pGe/Si junction with an illumination area same as the 0.1 μm^2 germanium gate, the photocurrent would be

$$I_{ph} = P \cdot \frac{A_{gate}}{A_{spot}} \cdot R_{diode} = 3e-3W \times 2e-4 \times \frac{0.1\mu\text{m}^2}{50\mu\text{m}^2} = 1.2nA. \quad (4.2)$$

in which R_{diode} is the responsivity of the diode device at 1550nm obtained earlier. Here, same quantum efficiency is expected in the Ge gate/Si channel junction as that in the heterojunction photodiode device since they are made of the same Ge-on-SOI substrate. The factor of A_{gate}/A_{spot} is added to count for the germanium gate being much smaller than the laser spot. Following this reasoning, *the “gain” introduced by the JFET design around the hetero pGe/Si junction is as large as $0.9\mu\text{A}/1.2n\text{A} = 750$!* In other words, if the quantum efficiency of hetero pGe/Si had not been that poor due to the pathetic quality of the germanium film, the CW responsivity of the Photo-Hetero-JFET would have been much greater than the apparent $3 \times 10^{-4} \text{ A/W}$.

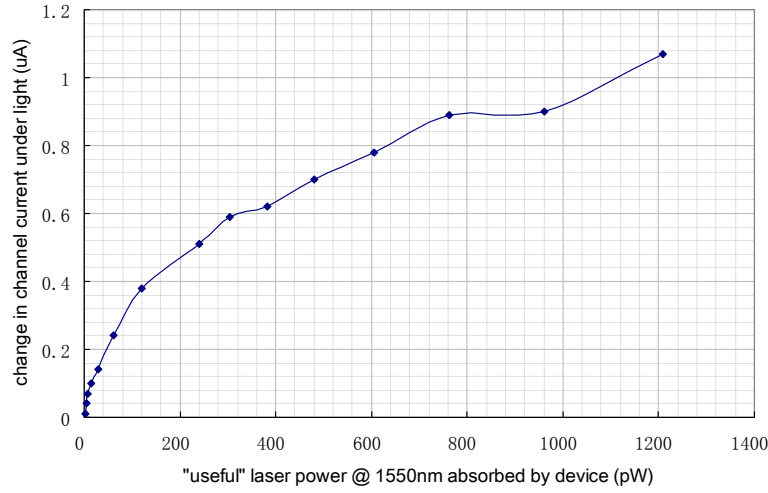


Fig.4-8 change in channel current with increase in “useful” laser power absorbed

To correct for the limited quantum efficiency that the poor quality of the germanium film offers, a plot of change in channel current ΔI versus the “useful” light power absorbed P_{eff} is presented below in Fig.4-8. The “useful” light power absorbed refers to the portion of the light absorbed that contributes to generating the collectable photocarriers in the heterojunction. From Fig. 4.8, one can find that, for 600pW light absorbed that generates all “useful” photocarriers, a current change in the channel is 0.8 μ A. This corresponds to a responsivity of 0.8 μ A/600pW=1333A/W! Again, this demonstrates the potential great sensitivity that the Hetero-Photo-JFET can achieve if the quality of material allows.

4.2.2 Time-resolved transient response

Since the Hetero-Photo-JFET is intended to be employed in future chip-level optical links, it has to provide optical gain at high modulation speed in order to be useful. Time-resolved measurement is then performed on the Hetero-Photo-JFETs. The schematic of the experimental set-up is shown in Fig.4-9. The optical set-up for focusing and aligning the incident light onto the submicron gate is almost the same as that in the set-up for continuous-wave illumination, except that a mode-locked laser at 1550nm is used instead of a CW one. A drain-to-source bias of 0.5V is again applied through the inductive (DC) arm of the bias-tee to the Photo-Hetero-JFET which is bonded on the high-speed chip carrier. The transient change in channel current is then sensed through the capacitive (AC) arm of the bias-tee, amplified by a high speed amplifier if needed, and fed to a 60GHz sampling oscilloscope. In the meantime, a picoammeter is connected in series in the DC arm of the measurement circuit to sense the average change in channel current.

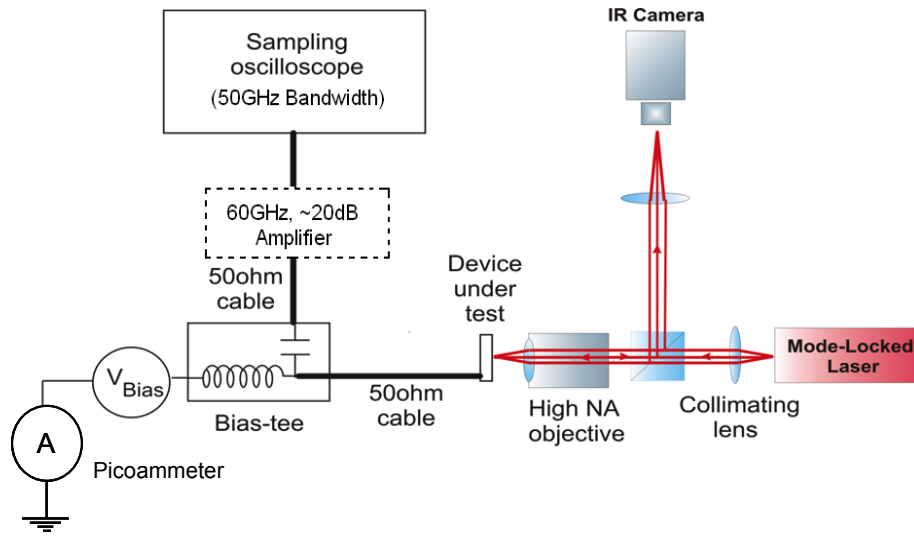


Fig.4-9 Schematic of the time-resolved measurement set-up with the Photo-Hetero-JFET.

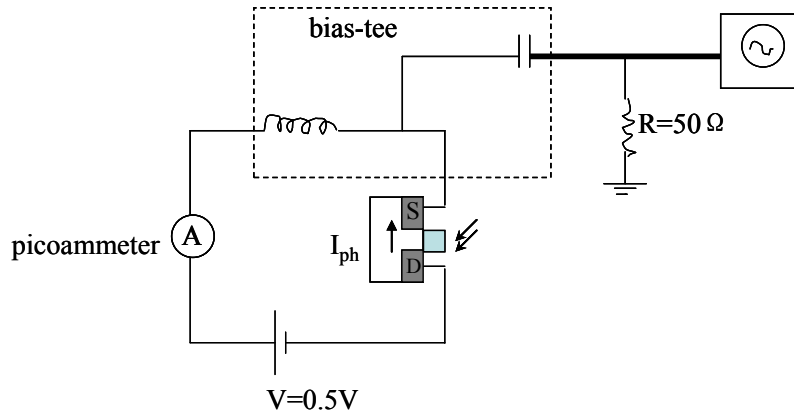


Fig.4-10 Circuit diagram of the time-resolved measurement on the Photo-Hetero-JFET

Note that the AC arm is impedance matched to 50Ω throughout the circuit (see Fig.4-9). This impedance is important in determining the output voltage seen by the oscilloscope. As will be explained in the later sections, the expected change in channel current in the Photo-Hetero-JFETs under such illumination condition is on the order of a few μA . Therefore the voltage seen at the 50Ω load is only of the order of a few $100\mu V$. Owing to the low level of the signal, the SNR is improved by extensively averaging the output of the oscilloscope using an externally connected computer ($\sim 400,000$ waveforms are used in each average). The noise is further reduced by employing a Faraday cage around the sample together with the focusing optics in order to shield it from external parasitic sources.

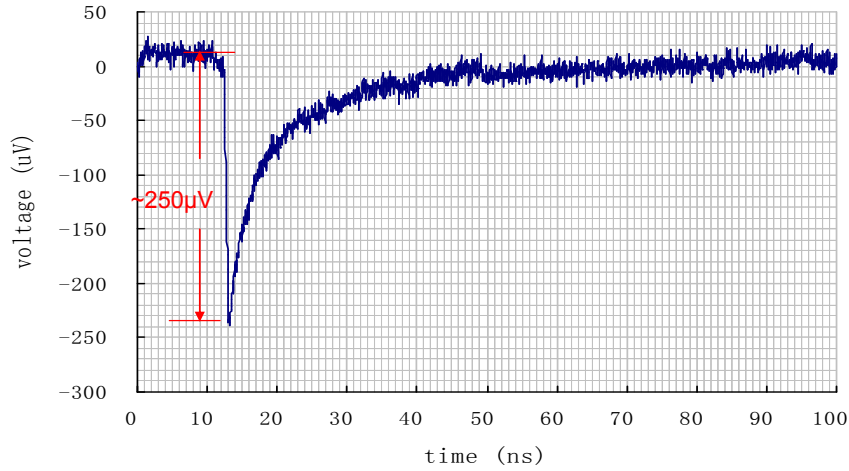


Fig.4-11 Time-resolved response displayed on the sampling oscilloscope of the Photo-Hetero-JFET to mode-locked 4ps pulse at 1.55 μ m with no amplification. The waveform data is averaged by 4096(oscilloscope averaging) \times 100(external computer averaging) = \sim 4,00,000 times.

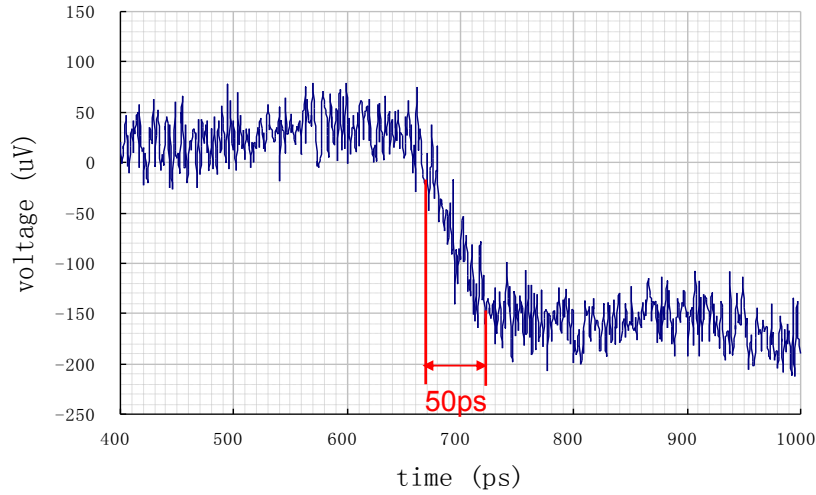


Fig.4-12 Zoomed-in picture of the rising edge of the time-resolved response with no amplification. The waveform data is averaged by 4096(oscilloscope averaging) \times 5 (external computer averaging) = \sim 20,000 times.

Transient response of the Hetero-Photo-JFET with 100nm gate length under pulsed light is shown in Fig.4-11. The light source is a mode-locked laser at the wavelength of 1550nm, which produces light pulses of 4ps duration with the rep rate of 10MHz. Its average power is 3mW so the peak power within one pulse is as big as 75W (if we assume the pulse is a square wave in time). Fig.4-11 shows the time-resolved response over 100ns, which is the period between adjacent laser pulses. One can see that the risetime seems to be very sharp in this time scale, whereas the tail of the response is quite

long. A zoomed-in picture at the rising edge of the transient response shown in Fig.4-12 indicates that the rise time sensed by the oscilloscope is $\sim 50\text{ps}$. The rise time represents a fall in voltage due to the way the bias circuit is set up. When light is incident on the gate, the resistance of the channel decreases and a spike of current goes through it. But this current goes through the 50Ω load from ground to positive, thereby causing a voltage drop to be recorded by the oscilloscope.

Note that the zoomed-in plot is much noisier. This is because the number of external averages taken of the signal in this time scale ($\sim 20,000$) is much less than that when the response over 100ns is taken ($\sim 400,000$). The reason that more intensive average of the zoomed-in signal cannot be obtained is that, jitters between each oscilloscope-averaged waveform (of 4096 waveforms) taken by the external computer at the timed instances can seriously smear out the originally sharp risetime hence resulting in a broadened unreal rising edge.

Since the change in channel current is fed into the oscilloscope which is a 50Ω load, the voltage presented on the oscilloscope is actual transient photocurrent times 50Ω . Also, from the picoammeter connected in series in the DC arm of the circuit, it is seen that the average current change under the pulsed laser is $\sim 0.8\mu\text{A}$ (from $35.6\mu\text{A}$ to $36.4\mu\text{A}$). Taking all those into consideration, the plot for the complete transient current change (ac plus dc components) over 100ns should be Fig.4-13. Note that the peak amplitude of the photocurrent is $\sim 5\mu\text{A}$.

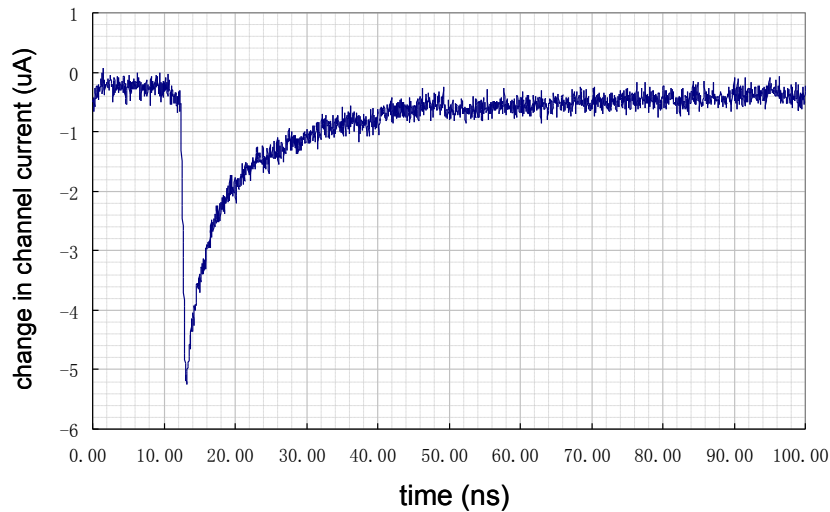


Fig.4-13 The total transient current change in the Photo-Hetero-JFET channel over one pulse period

4.2.3 Rise time of Transient Photoresponse

The bandwidth of a photodetector is determined by the speed with which it responds to variations in the incident optical power. Therefore, the concept of rise time T_r is introduced to define the time over which the current builds up from 10 to 90% of its final value when the incident power is changed abruptly [96]. Clearly, rise time T_r depends on the time taken by electrons or/and holes to travel to the electrical contacts, i.e. the transit time τ_{tr} . It also depends on the response time of the electrical circuit used to process the photocurrent, i.e. RC time τ_{RC} . Usually a complete mathematic description of rise time [96] is

$$T_r = (\ln 9)(\tau_{tr} + \tau_{RC}) \approx 2.2(\tau_{tr} + \tau_{RC}),$$

where the transit time is added to τ_{RC} because it takes some time before the carriers are collected after their generation through absorption of photons.

Here in the time-resolve measurements done on the Photo-Hetero-JFETs in response to 4ps laser pulses, as one can see in Fig.4-12, the rise time observed on the oscilloscope is 50ps. Since the transit time for electrons in Photo-Hetero-JFETs should be the sum of the time that photo-electrons in germanium “diffuse” to the gate/channel interface τ_{diff} (note that it is not appropriate to describe the transport of electrons in germanium with the model of diffusion for the reasons mentioned earlier; but we used “diffusion” here just to differentiate it from the drift motion of electrons in the channel), and the time for a gate-induced electron to traverse the channel τ_{drift} , i.e.

$$\tau_{tr} = \tau_{diff} + \tau_{drift}.$$

Since there’s hardly any “diffusion” of photocarriers in germanium,

$$\tau_{tr} \approx \tau_{drift}.$$

In a JFET with channel length of 100nm and a drain-to-source bias of 0.5V, the electrons drift at the saturation velocity v_{sat} , which is 10^7 cm/s. So the transit time of channel electrons in this photodetector is about

$$\tau_{tr} = L_{channel}/v_{sat} = 1\text{ps},$$

which is much smaller than the observed rise time. Clearly, the rise time of the transient response of Photo-Hetero-JFET is not limited by τ_{tr} , but τ_{RC} . A quick examination of the measurement circuit which is presented by a simplified schematic in Fig.4-10 reveals that the 50Ω SMA cable is one of the bottlenecks that prevent the risetime from being as sharp as the extremely short transit time would allow. It is known that a best SMA usually has a bandwidth of ~20GHz, as the bandwidth of a RC circuit is given by

$$\Delta f = (2\pi \cdot \tau_{RC})^{-1} = (2\pi \cdot T_r / \ln 9)^{-1},$$

the fastest possible rise time T_r that corresponds to the bandwidth of the SMA cable would be ~20ps. Moreover, recall that the Au wires that bonds the source/drain contact pads to the chip carrier are only ~1mm in length, which means that they each have wire inductance of ~1nH. Hence the response delay caused by the inductance is negligibly

small, which is

$$\Delta\tau = \frac{L}{R_{load} + R_{channel}} = \frac{2nH}{50\Omega + 14k\Omega} = 0.14\text{ ps}.$$

Therefore it is proven that the rise time of the Photo-Hetero-JFETs is limited by the RC time of the external electrical circuit that senses the transient photoresponse, specifically by the bandwidth of the SMA cables. *It is not inherent in the photodetector itself!*

It is reasonable to expect when the Photo-Hetero-JFET is integrated in the real chip-level high-speed optical link with all other components ideally optimized, the response time of this photodetector should approach its transit time, which is 1ps. This implies that the Photo-Hetero-JFETs can potentially be employed in the applications with bandwidth of 100GHz. However, to achieve the required bandwidth of 40GHz for the photonic circuits in current commercial products, the risetime of photodetector should then be less than 9ps, which is readily achievable in this Photo-Hetero-JFET with 100nm channel. Thus in our lab setting, it is not necessary to go to large expense to replace the SMA cables with fancy but pricy ultra-fast cables just to show that the photodetector can indeed have risetime of a few pico-seconds. This is also for the reason that, the main problem in high speed Photo-Hetero-JFETs stem from the long fall time.

4.2.4 Fall time of Transient Photoresponse

Although a sharp rise time presented in transient photoresponse of the Hetero-JFET photodetector is very encouraging, a long tail (with fall-time of ~26ns) that follows indicates a practical problem the photodetector faces before it can be regarded as fast.

In fact, long fall time is normally expected in the transient response of devices whose operating mechanisms are based on trapped charges. In a physical picture of the Photo-Hetero-JFET, after the laser pulse is turned off, photo-holes trapped at the interface which induce the channel modulation, need to decay away for the photoresponse to disappear. In other words, the voltage built up across the junction needs to decay away. So the lifetime of trapped holes or the relaxation time of photo-voltage on the gate determines the fall-time of the photoresponse. As the germanium gate is kept floating, there's no external circuit route for the trapped holes on this side of the heterojunction to go to relax the photo-voltage. Therefore the trapped holes that charge the junction capacitance during the pulse (Fig.4-14(a)) should only discharge through the resistance of the heterojunction (Fig.4-14(b)). Please note that, the discharging time of this heterojunction is essentially the time it takes for the trapped holes at Ge/Si interface to recombine, i.e. the dielectric relaxation time.

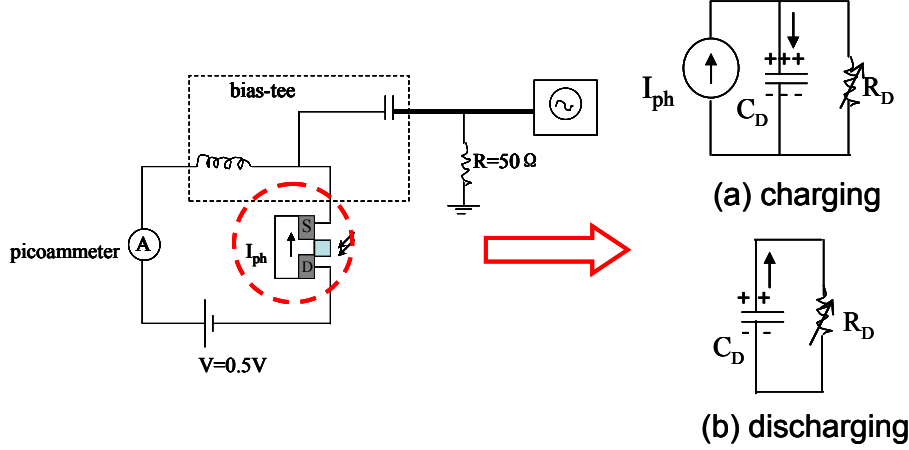


Fig. 4-14 Replot of the circuit diagram of the time-resolved measurement, showing the equivalent circuit of (a) charging and (b) discharging the junction capacitance.

4.2.5 Discharging of the heterojunction capacitance

The circuit model of the heterojunction that describes charging of the junction capacitance during the pulse by photocurrent and discharging of the capacitance after the pulse are shown in Fig.4-14. R_D is the junction resistance, so it is a variable resistance that follows the junction IV curve (Fig.4-4), i.e.

$$R_D = \left(\frac{dI_D}{dV} \right)^{-1} \cong \left(\frac{q}{\eta kT} I_D \right)^{-1} = \frac{\eta kT}{q I_D}.$$

The junction capacitance C_D is also a non-constant quantity that varies with depletion width W_D which is in turn a function of junction voltage. To get a time-resolved plot of trapped charges Q_{ph} being discharged through the heterojunction, we can analyze the circuit in Fig. 4-14 and solve for the photo-voltage V_{ph} . Before we do that, the following assumption is made: As C_D varies inversely proportional to W_D which only changes linearly with $(V)^{1/2}$ but R_D varies exponentially with V , C_D is first kept as a constant in the circuit to prevent the analytical solution from becoming unnecessarily complicated.

Assume that when the optical pulse is turned off, the initial voltage on the junction is V_i . The current I that discharges the junction capacitance is the same current that goes through the diode resistance. The set of differential equations that describe the discharging process is then

$$V = V_i - \frac{\int I dt}{C_D}$$

and

$$I = I_0 \left(\exp\left(\frac{qV}{\eta kT}\right) - 1 \right),$$

which is the diode equation. Solving for junction voltage V , we obtain the following analytical solution (the solution is verified by reference [97]):

$$V(t) = -\frac{\eta kT}{q} \ln[1 - (1 - \exp(-\frac{qV_i}{\eta kT})) \cdot \exp(-\alpha t)], \quad \alpha = \frac{qI_0}{\eta kTC_D}.$$

For the Photo-Hetero-JFETs, C_D is taken to be the capacitance of the pGe/Si junction when fully-depleted,

$$C_D = \frac{\epsilon_{Si} A_{gate}}{W_D} = \frac{1.04 \times 10^{-12} \times 0.1 \times 10^{-8}}{2 \times 10^{-5}} = 52 aF \text{ (atto-farad)}.$$

The diode equation for pGe/Si junction is obtained previously from the characterization of heterojunction diode. Now for the Ge gate/Si channel junction of $100\text{nm} \times 1\mu\text{m}$ in size, the diode equation becomes

$$I = 1.41 \times 10^{-13} (e^{\frac{qV}{1.14kT}} - 1) \text{ Amp}, \quad (4.3)$$

so $I_0 = 1.41 \times 10^{-13} \text{ A}$, and $\alpha = 6.302 \times 10^4$.

The possible initial voltage V_i that is generated by the big laser pulse on the junction capacitance can be estimated by assuming the same responsivity for the gate/channel heterojunction as the CW responsivity of the diode device characterized earlier, $R = 2 \times 10^{-4} \text{ A/W}$. This also means we assume the same quantum efficiency, which is very unlikely since with a pulse of much bigger intensity the recombination of photocarriers would increase significantly and thereby reduce quantum efficiency. For an instantaneous power of 75W during the pulsewidth, the instantaneous photocurrent is then $30\mu\text{A}$ (note that a factor of A_{gate}/A_{spot} should be included too). If we further assume that the Fermi-levels of the junction response immediately to photocurrent and present voltage that follows the diode equation (4.3), the voltage estimated should be $\sim 0.5\text{V}$. This voltage is not possible as it is even bigger than the built-in voltage of junction, $V_{bi} = 0.405\text{V}$! However, since the real quantum efficiency under pulsed illumination should be much worse than in the CW case, and also because carriers in the junction takes time to redistribute to establish a steady-state voltage described by the diode equation, the actual initial voltage will be much smaller than the estimated value and must also be smaller than the built-in voltage to be physical. Nonetheless, the previous estimate gives us an upper-bound value of the initial voltage V_i , which is 0.4V . By plugging all the parameters together with various values of V_i , the plot of the junction voltage V versus discharging time t_{dis} over 100ns range is shown in Fig.4-15.

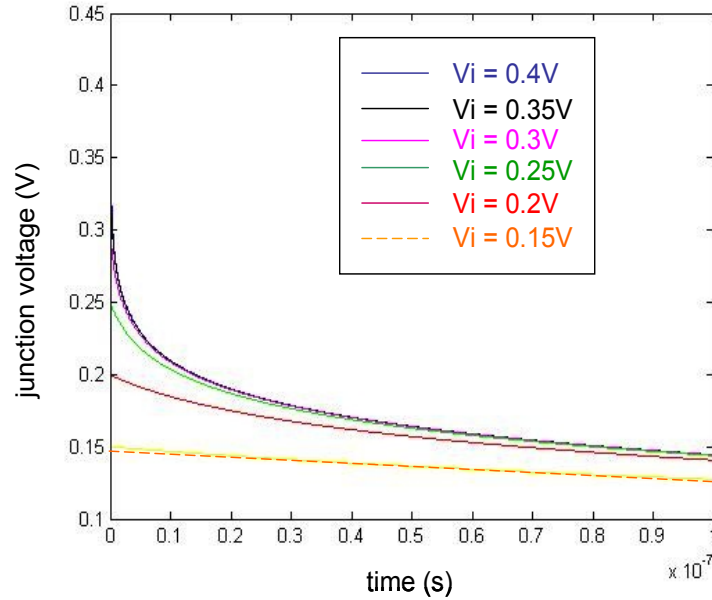


Fig.4-15 Discharging of junction voltages over time (100ns) through junction resistance with different initial voltages.

We see that only with a large initial voltage ($V_i > 0.25\text{V}$), the decay of junction voltage displays an initial sharp decrease. Recall that in the hetero-JFET photodetector, the junction voltage is the gate voltage V_g that works to decrease the depletion width and thereby increase the channel current I_{ch} , and the channel current I_{ch} of a JFET is roughly proportional to $(V_g)^{1/2}$. For the decay of I_{ch} to resemble the experimental decay observed in the time-resolved measurement (Fig.4-13), the decay of V_g must present an even sharper drop at the beginning than that in the experimental data. This would require the initial voltage built up on the gate, V_{ig} , to be large. As indicated in Fig.4-15, V_{ig} needs to be larger than 0.25V for the initial decay to appear sharp at this time scale (over 100ns). For a complete description of junction voltage decay in the discharging model, a zoomed-in plot showing various curves over the initial 1ns is also presented in Fig.4-16. One should bear in mind that the junction capacitance C_D actually decreases with the decay of voltage, which would result in the decay of the actual voltage, if compared to the case when C_D is constant, becoming increasingly faster with time.

As will be revealed later in the thesis, the photovoltage that generated across the gate/silicon heterojunction under the pulsed illumination is never as large as 0.25V. Therefore, although the capacitive discharge model sounds perfectly physical and valid, and even encouragingly presents the possibility to match the tail observed in the time-resolved measurement, careful estimation proves that it only accounts for the excessive long falling trend after the initial sharp decrease. Other mechanisms than this capacitive discharge model are needed to fully explain the tail.

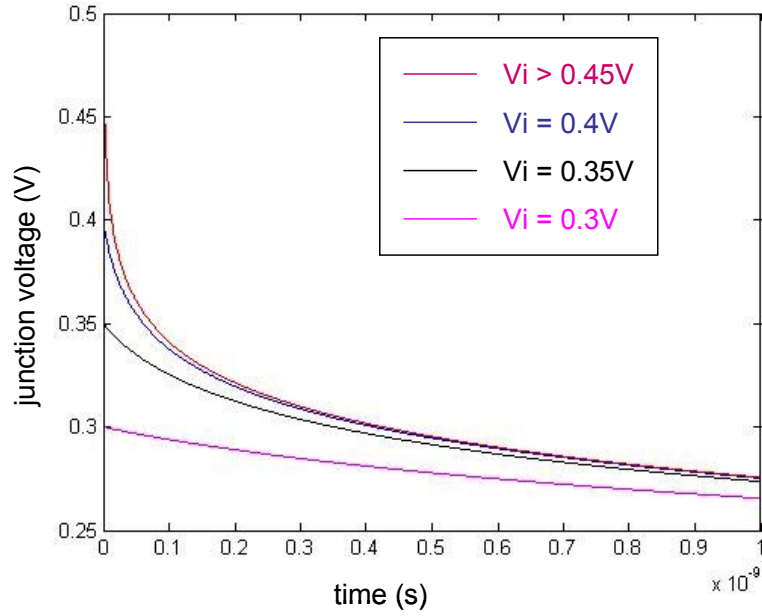


Fig.4-16 Zoomed-in plot of discharging of junction voltages over the first 1ns through junction resistance with different initial voltages.

At this stage, one question is raised up about the tail - whether the tail is inherent in the JFET photodetector being a device based on trapped charges, or is actually related to the charge transport property in the germanium even in the heterojunction diode configuration. With this reasoning, it is instructive to go back to the heterojunction diode device and study its transient response.

We'll leave the discussion for now on the fall time of the transient response of Photo-Hetero-JFETs, and will come back to it later since more experimental data needs to be obtained for completing the understanding of the tail.

4.3 Further analysis on heterojunction photodiode device

4.3.1 Time resolved transient response of diode devices

As already mentioned repeatedly in the thesis, it is worth emphasizing again that the physics happening in the p-Ge gate/Si channel heterojunction is what dominates the performance of the Photo-Hetero-JFET detectors. Therefore, it is of essential importance to fully characterize the heterojunction diode devices. In the organization of this chapter, DC performance of the diode devices is discussed first, and we come back to its transient response after some discussions on the transistor devices. The reason for this order of discussion is that, it is the actual order we did the various characterizations and it shows

how our understanding and reasoning developed along the line. It is our hope that with such organization, the readers can better grasp our line of logic in this research and understand this work more easily.

As mentioned in the previous section, to understand the tail of transient response of the transistor device better, it is necessary to characterize the transient response of the heterojunction diode devices under the same pulsed illumination. The measurement set-up is the same except for that now the device-under-test is the heterojunction photodiode (please refer to Fig.4-9). Furthermore, the bias across the photodiode is kept as zero, i.e. the short-circuit current of the diode is being probed. The equivalent circuit is presented in Fig.4-17.

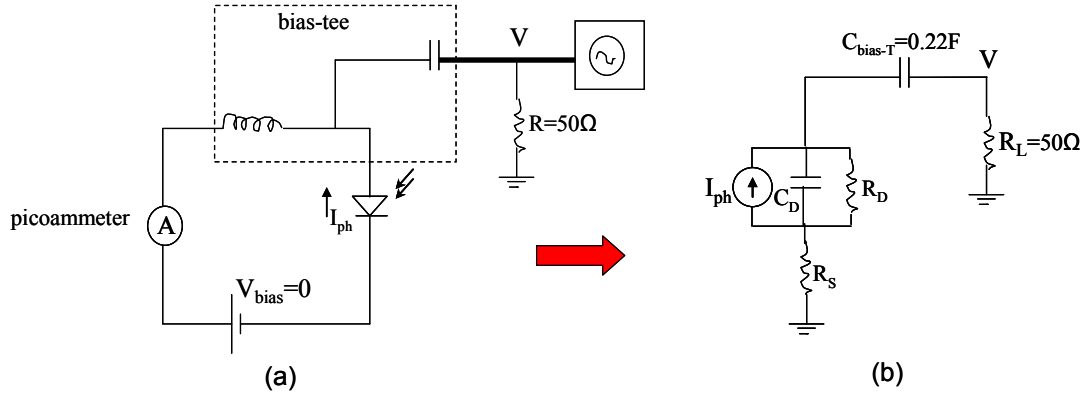


Fig.4-17 Circuit diagram of time-resolved measurement on the heterojunction diode device

The transient response of the heterojunction diode to the pulsed laser is shown in Fig.4-18. Much to our surprise, it presents a similar tail to that of the transient response of the transistor device. Since there's no gain present in the diode device, the response is quite weak. The transient photocurrent from the diode is sent through a 60GHz amplifier before it can be observed on the oscilloscope. The amplifier adds additional noise to the signal and that's why the transient response of the diodes shown in Fig.4-18 carries much more noise than that of the Photo-Hetero-JFETs. The voltage gain of the high-speed amplifier is ~ 20 , so the actual peak photocurrent is

$$I_{peak} = \frac{210\mu V}{20 \times 50\Omega} = 0.21\mu A.$$

It is also seen from the picoammeter that the average photocurrent of the diode under pulsed illumination is $\sim 0.31\mu A$. Similarly, the complete transient photocurrent (ac plus dc components) of the heterojunction over 100ns is plotted in Fig.4-19 in the same way as that of the Photo-Hetero-JFET is done in Fig.4-13. Please note that since the high-speed amplifier is a three-stage amplifier which inverts the polarity of the signal, the onset of the photocurrent in Fig.4-19 has a rising edge as opposed to the falling edge displayed on

the oscilloscope (Fig.4-18). Were it not for the amplifier, the photocurrent of the diode would go through the 50Ω load from positive to ground, and the waveform on the oscilloscope would be with a rising edge.

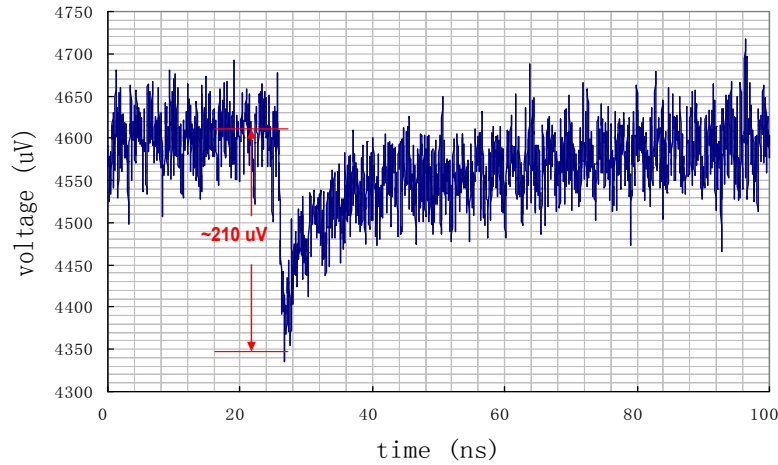


Fig.4-18 Time-resolved response displayed on the sampling oscilloscope of the heterojunction diode to mode-locked 4ps pulse at 1.55μm with voltage amplification of 20. The waveform data is averaged by 4096(oscilloscope averaging) x 100(external computer averaging) = ~ 4,00,000 times.

The examination of its rise time reveals that it is again limited by the bandwidth of the SMA cables. However, the long tail in the transient response is a bit unexpected out of the heterojunction device, but it answers the question raised at the ends of the last section - yes, the tail already exists in the photocurrent formed in the heterojunction! The presence of such a tail is surprising for the heterojunction diode but not for the Photo-Hetero-JFETs, for the reason that, the germanium gate is floating so there is no route for the trapped charges to leak in that open-circuit configuration; however the heterojunction diode is “short-circuited”, and thus there should be no problem for the photocarriers to escape. A further examination of the measurement circuit in Fig.4-17(b) suggests that there’s an RC-time associated with the decaying of the voltage on C_D through the series resistance R_s and the load resistance R_L , i.e.

$$\tau'_{RC} = (R_s + R_L) \cdot C_D$$

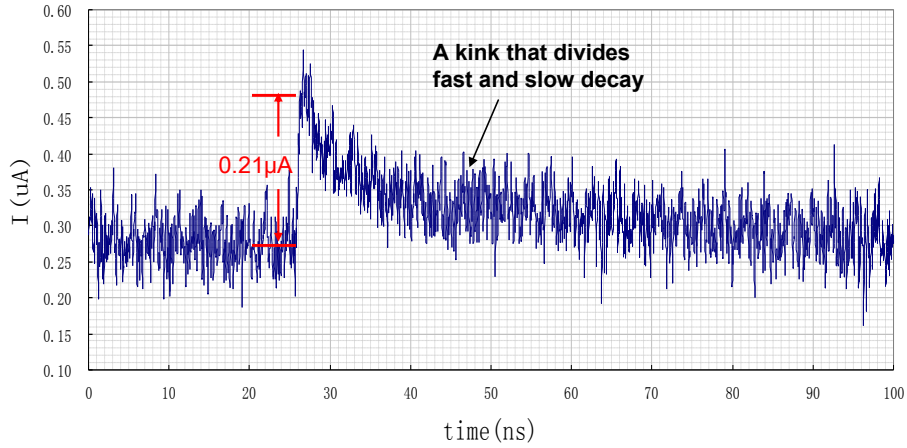


Fig.4-19 The total transient photocurrent in the heterojunction diode over one pulse period

The junction capacitance of the diode device with $400\mu\text{m} \times 400\mu\text{m}$ germanium mesa is

$$C_D = \frac{\epsilon_{Si} A_{gate}}{W_D} = \frac{1.04 \times 10^{-12} \times 1.6 \times 10^{-3}}{2 \times 10^{-5}} = 83.2 \text{ pF}.$$

The series resistance of the heterojunction is estimated from the forward IV curves (Fig.4-4) to be $R_s \sim 10\text{k}\Omega$. So τ'_{RC} is $\sim 830\text{ns}$. This is a very long relaxation time compared to 100ns , the time period between two adjacent pulses. This could explain the large dc component in the diode photocurrent in response to laser pulses. The voltage on the junction capacitance in this pulse period did not die away completely when the next pulse comes, of which the effect accumulates and forms the steady-state base current. However, such decay is on a very long time scale, and probably explains the slow decay shown after the kink in the tail (Fig.4-19), but not the fast decay on top of it. Please note that the onset of the photocurrent or the rising edge is not restricted to this RC time since the photocurrent simply goes to the 50Ω load with the capacitance in the bias-tee shorted.

Recall that the germanium film in the heterojunction diode is found to be very defective according to the unphysically small diffusion length estimated from responsivity measurements, and it is even suspected to be amorphous. It is highly possible that the transport of carriers in the germanium is “anomalous”, as opposed to drift and diffusion - normal transport models which are usually dominant in the ordered structure.

4.3.2 Dispersive transport

A more normal name for the “anomalous transport” is called dispersive transport. It is usually used to explain the pulsed photoconductivity observed in disordered samples [98-102]. In ordered semiconductor with well-defined crystalline lattice structure and properties such as carrier mobility, the photocurrent pulse will ideally look like a perfect

square wave. Due to carrier diffusion, the actual drop-off in current presents rounded leading and trailing edges because the charged carrier pulse spreads out as it propagates. This “relatively innocuous but well-understood form of dispersion” [101], known as diffusion, occurs from random walk excursions as the carrier makes its way across the transit width. Either drift or diffusion in an ordered semiconductor brings little dispersion to the transient photocurrent.

However, the truly anomalous behavior is observed in amorphous versions of semiconductors. The narrow pulse of carriers seen in an ordered sample now shows a large spread in its concentration profile as it makes its way between contacts (see Fig.4-20). This results in a highly dispersive transient photocurrent trace. Fig.4-21 shows an example of the photocurrent trace observed by time-resolved measurements on As_2Se_3 by Scharfe [100]. It is seen that the current spike immediately after the onset of the short light pulse is followed by a soft “plateau” of the current level, then a transition region and finally a ubiquitous long “tail”. As Harvey Scher and Elliott Montroll pointed out in their famous work in dispersive transport [100], these distortions to the ideal response indicate some statistical process causing a spread in the transit times (or a distribution in surface release times). The long tail represents “the dribble of the slow carriers”, and the shoulder region or on-set of the tail suggests the transit time t_r , although, one often does not even see a shoulder. Scher and Montroll first described this behavior of the pulsed photocurrent theoretically using the stochastic model taking into account the wide distribution of hopping probability between neighboring sites in which the carriers are localized. Based on their proposed “distribution of hopping time”, $\psi(t) \sim \text{const} \times t^{-(1+\alpha)}$, $0 < \alpha < 1$, they derived the current variation to be $I(t) \sim \text{const} \times t^{-(1-\alpha)}$, $t < t_r$ and $I(t) \sim \text{const} \times t^{-(1+\alpha)}$, $t \gg t_r$. Their derived result has found supports in many experimentally observed evidences (see ref. 9,11,21 in [100]). Fig.4-22 is one that they quoted, which clearly shows the slopes of $-(1-\alpha)$ and $-(1+\alpha)$ in the $\log I - \log t$ plot with $\alpha = 0.45$.

Dispersive transport was also explained by the multiple-trapping model by Rudenko and Arkhipov [103], Schmidlin [104] and Noolandi [102]. In these works the transport of charge carriers is considered in terms of “unestablished thermal equilibrium between the mobile carriers and those localized in energy-distributed traps”. Thus, the dispersive transport of charge carriers has been interpreted physically as “a transient process, following the photocurrent pulse, of the setting in of a thermodynamic equilibrium between the conduction band and the energy-distributed traps”[98]. Noolandi[105] also proved that the model of multiple trapping is equivalent to the continuum limit of the continuous-time-random-walk description of anomalous dispersion developed by Scher and Montroll. He expressed the hopping time distribution function $\psi(t)$ in terms of the parameters of the multiple-trapping model.

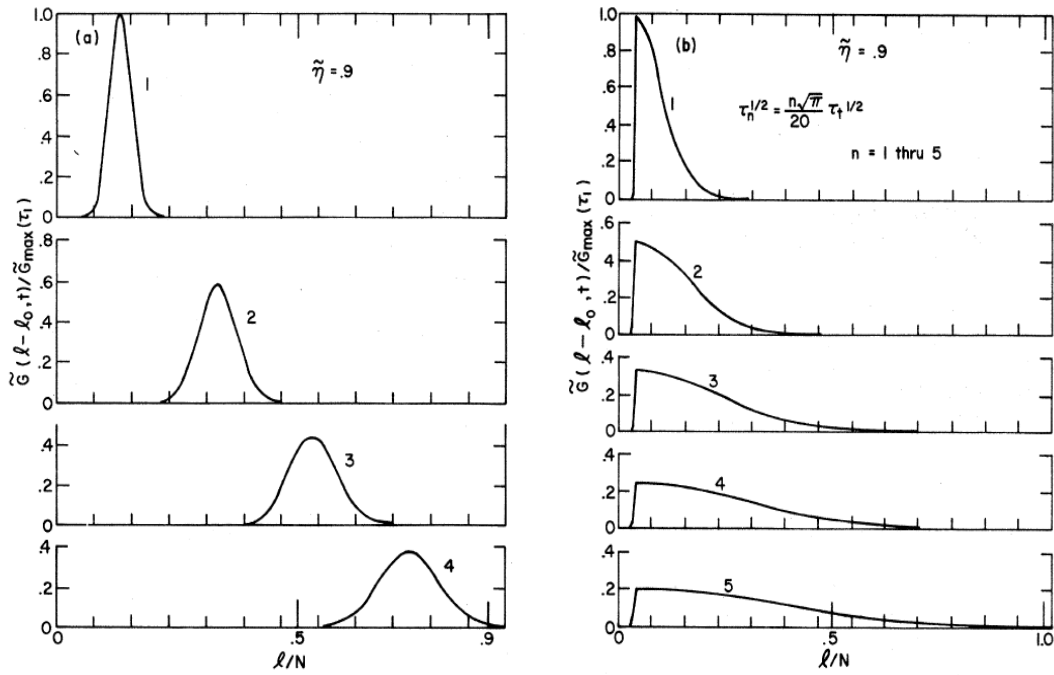


Fig.4-20 (a) normal transport

(b) dispersive transport (reproduced from ref. [100])

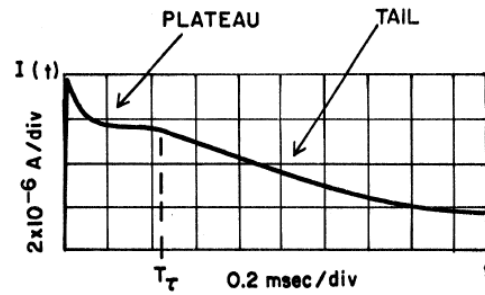


Fig. 4-21 example of highly dispersive photocurrent trace observed by time-resolved measurements on As_2Se_3 by Scharfe (reproduced from ref. [107])

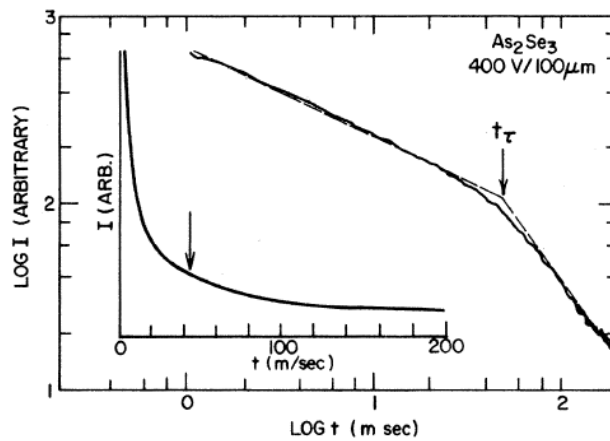


Fig. 4-22 Trace of an electronically produce log I-log t plot for As_2Se_3 by Pfister. The dashed lines

have slopes of -0.55 and -1.45, respectively. The inset shows trace of the oscillogram of I vs. t. (reproduced from ref. [108])

The transient photocurrent trace obtained for our heterojunction diode device resembles that in Fig.4-21, and could be of characteristic of dispersive transport. Owing to large lattice mismatch between germanium and silicon substrate and non-optimized growth condition on SOI wafers, the evaporated germanium is very susceptible to having large density of electronic defect states across the bandgap. Normally, the defect states around the mid bandgap between the demarcation levels are considered efficient recombination centers, and those near the band-edges are traps that, in thermal equilibrium with conduction bands or valence bands, capture and release carriers [85]. As there is zero bias applied across the heterojunction, the photocarriers generated by the 4ps pulse are not much driven by field-assisted drift. Those photocarriers that have survived all kinds of recombination - geminate recombination as well as recombination via localized states - are very like to be captured by traps with various lifetimes. Upon being released from a trap into conduction band or valence band, the carrier can still be captured by another trapping center before it gets freed again. Such a process repeats until the carrier reaches the contact and gets collected as photocurrent. In a sense, the transport of this carrier can well be described by hopping between multiple trapping sites in a statistical manner. Such exchange of carriers between traps and bands disturbs the normal carrier transport and results in large dispersion in carrier transit time. Therefore, in the transient response of the diode device, only photocarriers with effective transit times smaller than 100ns (duration between adjacent laser pulses) make their presence in the current pulse, while others “buried” in the baseline of the photocurrent.

Although multiple traps can be involved in the transport of one carrier, a simplified model can be proposed in which only “one effective trap” with a certain lifetime is assumed to encompass the effects of all the traps that are physically involved, and that carrier only dwells in this trap for duration of lifetime τ before it's freed and collected. Thus in this setting, the transient photocurrent component contained in the pulse is contributed by photocarriers once trapped in traps with lifetimes smaller than 100ns. Integration of the transient photocurrent over 100ns reveals that the photocarriers in these fast traps are $\sim 25,000$. This corresponds to a concentration of occupied fast traps in the heterojunction of $1.5625 \times 10^7 / \text{cm}^2$. To conclude, the long tail in the transient photoresponse of the heterojunction device is attributed to dispersive transport of photocarriers in the defective germanium, described either by statistical hopping or trapping-and-detrapping via traps.

4.3.3 Continued discussion of fall-time

Now is good time to go back to the discussion of the fall time in the transient response of the Photo-Hetero-JFETs. Since the dwelling of photocarriers in traps can explain the spread in carrier “transit time” in germanium, it also accounts for the prolonged photoconductivity modulation in the transistor devices as seen in the long tail. In the frame of simplified “one-trap” model, the transient current trace of diode devices suggests the concentration of traps with different effective lifetimes, while in the transient response of the transistor devices, the current trace is indicative of the total sum of occupied traps at each time instant. So if illumination intensity normally incident on the germanium mesa had been the same for both diode and transistor devices, the current trace on the falling edge of the transistor device would have been the integral of that of the diode device. However, the light intensity on the nano gate ($0.1\mu\text{m}^2$ gate, under $50\mu\text{m}^2$ laser spot) in the transistor is 3200 times stronger than that on the germanium mesa (0.0016cm^2 mesa and laser spot). This difference results in a 3200 fold larger density of photocarriers generated in the transistor than in the diode. However, the complications in the interaction of traps with conduction/valence band (exchanging carriers between them) prevent the effects of dispersive transport to scale linearly with the carrier density, thereby the supposed proportional relation between the two transient plots are not seen.

4.4 Modeling of the time-resolved response of Photo-Hetero-JFETs

Now that both rise time and fall time of the transistor transient response are well-explained, various amplitudes in the transient photocurrents are to be closely examined and analyzed. The organization of this section goes as the following: first, several models proposed for interpretation of Photo-Hetero-JFETs are presented, some of which have already been touched upon in our previous discussions; then, the attempts to fit the experimental results into the frames of these models are made which will be described following the “problem-diagnosis-solution” order, as how we tackled the issue of fall time earlier in the chapter; finally, the model or combination of models that best represents the physics of Photo-Hetero-JFETs is chosen, and its differences and connections with the other models are discussed.

4.4.1 Physical models for Photo-Hetero-JFETs

As the Photo-Hetero-JFET device is essentially a junction field-effect-transistor in which a floating germanium optical gate replaces the traditional electrical gate, it is natural to use the JFET transistor model to interpret the device, except that the gate voltage V_g is implicit in the case of an optical gate. There are two proposed ways to extract the effective gate voltage: one is the open circuit voltage when the heterojunction is treated as a photovoltaic cell; the other is by estimating the decrease in depletion width under the effect of electrostatic coupling from trapped charges in the germanium gate.

I. JFET transistor with photovoltaic voltage model

In this model, the pGe gate/Si channel heterojunction is modeled as an open-circuit photovoltaic cell. The open-circuit voltage V_{oc} across this cell under near-infrared illumination is the forward gate voltage V_F that decreases depletion in the silicon channel. If the diode equation for dark I-V curve is

$$I_{dark} = I_0 \left(\exp\left(\frac{qV}{\eta kT}\right) - 1 \right),$$

the total current of the junction in light is then

$$I_{total} = I_0 \left(\exp\left(\frac{qV}{\eta kT}\right) - 1 \right) - I_{ph},$$

which shows on the I-V plot as simply shifting the dark I-V plot down by I_{ph} . In a cell with quantum efficiency of η and under photon flux of ψ , $I_{ph} = e\eta\psi$. The open circuit voltage V_{oc} is therefore found by setting $I_{total} = 0$, i.e.

$$V_{oc} = \frac{\eta kT}{qV} \ln\left(\frac{I_{ph}}{I_0} + 1\right). \quad (4.4)$$

The photocurrent is estimated from the photon flux and quantum efficiency of the heterojunction diode, i.e.

$$I_{ph} = q\varphi\eta_{diode} = q \frac{P}{h\nu} \eta_{diode}.$$

In a JFET transistor, the channel current I_{ch} is derived to be [96]

$$I_{ch} = \frac{W\mu_n q^2 N_D^2 t^3}{6\epsilon_{Si} L} \left[\frac{3}{t^2} (h_D^2 - h_S^2) - \frac{2}{t^3} (h_D^3 - h_S^3) \right]. \quad (4.5)$$

where t is the thickness of the entire silicon layer, L is the silicon channel length, W is the channel width and N_D is the channel doping. In addition, μ_n is the electron mobility and ϵ_{Si} is the permittivity of silicon. h_D and h_S are the depletion widths at the drain and source ends, respectively-

$$h_D = \sqrt{\frac{2\epsilon_{Si}(V_{bi} + V_D - V_G)}{qN_D}} \quad \text{and} \quad h_S = \sqrt{\frac{2\epsilon_{Si}(V_{bi} + V_S - V_G)}{qN_D}}.$$

in which V_G is the voltage applied on the gate, and in the frame of this model, V_{oc} .

For the Photo-Hetero-JFET with 100nm channel under a drain-to-source bias of $V_{DS} = 0.5V$, the electron velocity reaches saturation velocity $v_{sat} (= 10^7 \text{cm/s})$, so an effective mobility $\mu_{eff} = v_{sat}/E_{channel}$ is assumed in order for Eqn.(4.5) to be applicable. To fit the phototransistor dark current of $35.6\mu A$ with Eqn.(4.5), the average channel doping is then found to be $4.02 \times 10^{16} \text{cm}^{-3}$.

A simplified JFET model does not take into account the non-uniform depletion profile caused by the drain-to-source bias – there's more depletion at the drain side due to larger reverse bias across the junction at this end. The channel current is derived to be

$$I_{ch} = qv_{sat}WN_D(t - W_D), \quad (4.6)$$

and W_D is the depletion width under the gate bias V_G , i.e.

$$W_D = \sqrt{\frac{2\epsilon_{Si}(V_{bi} - V_G)}{qN_D}}.$$

The average channel doping is estimated from this simplified JFET model to be $3.15 \times 10^{16} \text{cm}^{-3}$. When the continuous-wave 1550nm laser of 3mW is incident on the germanium gate of the Photo-Hetero-JFET, the photocurrent generated is calculated from Eqn.(4.3) to be 1.2nA. The responsivity of the heterojunction itself R_{junction} is taken to be the responsivity value that obtained for the big area diode device, 2×10^4 , multiplied by the factor of $A_{\text{gate}}(0.1 \mu\text{m}^2)/A_{\text{spot}}(50 \mu\text{m}^2)$. The open circuit voltage generated across the junction is obtained to be 0.2579V via Eqn.(4.4), in which I_0 is $J_0(1.41 \times 10^{-4} \text{A/cm}^2)$ times A_{gate} and η is the diode quality factor 1.14. However, when we plug this open-circuit voltage value together with all other parameters of the Photo-Hetero-JFET into both JFET current equations Eqn.(4-5) and Eqn.(4-6), we get a channel current of 57.06μA and 61.53μA, respectively. Both values are much larger than the real experimental observed value of 36.5μA (35.6μA dark current plus 0.9μA CW photocurrent).

In an attempt to explain this discrepancy, we want to re-examine the performance of a JFET under forward bias. Most JFET transistors are operated with the gate voltage in the reverse direction. Even for JFETs operated in the enhancement mode, the variation in the gate voltage is done by decreasing the reverse bias across the junction. It is not usually recommended to forward-bias the gate-source junction as substantial current will flow and the junction is not designed to handle that. Since the estimated photovoltage on the germanium gate of the hetero-JFET is quite large, the junction current might have overwhelmed any change in the channel current caused by depletion modulation. It looks like under forward bias, the junction-FET is better modeled as two back-to-back diodes in parallel with the channel resistance (see Fig.4-23. R_G , R_S and R_D are contact resistances of the three terminals). The channel resistance is modeled as a variable resistor whose value changes with the junction bias. So when the gate bias is large, the gate-to-source junction resistance (even the gate-to-drain junction resistance) becomes very small and thus the channel resistance is shorted. In order to understand what regime that the photo-JFET could be operating in, JFET transistors with larger junction area ($400 \mu\text{m} \times 400 \mu\text{m}$), but of almost the same structure as that of Photo-Hetero-JFETs, are fabricated on Ge/SOI substrate. One difference is that electrical contact is deposited on the germanium gate so that we can probe the source-to-drain current of the JFET with

well-defined electrical voltage applied on the gate.

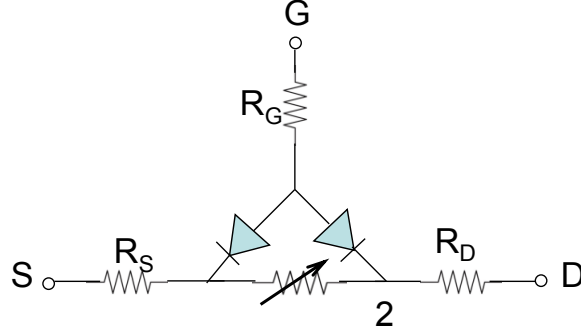


Fig.4-23 Back-to-back diode circuit model of a JFET transistor

Differential resistance measurement is performed on the big JFET device to probe the resistance between the source and drain terminals when a range of electrical voltages are applied on the germanium gate. The semi-log plot of the resistance between 1 and 2 (Fig.4-23) versus the gate bias is shown in Fig.4-24. With the gate voltage larger than 0.15V, the resistance across the channel decreases exponentially with the voltage, clearly indicating that the transistor is operated as two diodes and the channel depletion modulation goes unnoticed. When the gate bias is smaller than 0.15V, the transistor operates as normal JFET and the resistance is the channel resistance modulated by the gate voltage. The resistance range in the JFET regime goes from 10k Ω to 6.3k Ω for the big JFET device. With this, we examine the drain-to-source resistance of the Photo-Hetero-JFET with 100nm gate length, which only changes from 14.04k Ω in dark to 13.70k Ω when the 3mW CW 1550nm laser is incident. This small range of resistance change suggests that the Photo-Hetero-JFET does not reach the two-diode exponential regime but indeed stays in the operation regime of a normal JFET.

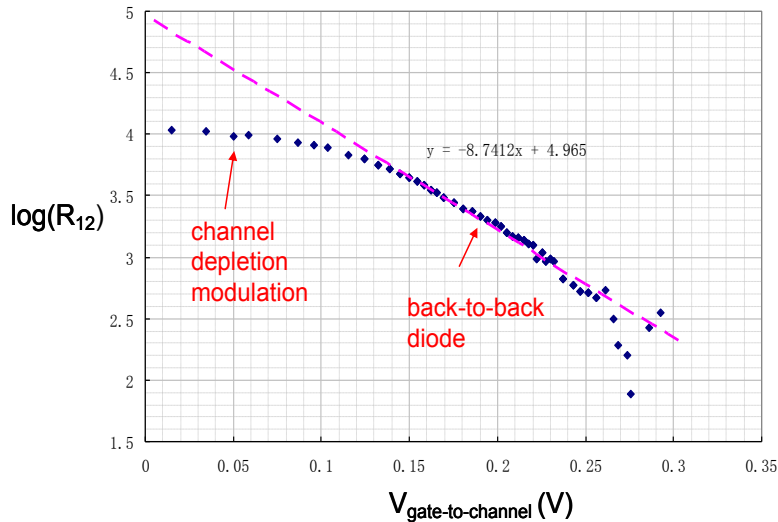


Fig.4-24 Semilog plot of differential resistance of the big JFET channel vs. the gate voltage.

One has to notice that in the previous estimation of the open-circuit voltage ($V_{oc}=0.2579V$) for the Photo-Hetero-JFET device under the CW laser, photoresponsivity of the heterojunction was assumed in a way that the same recombination probability P_{recom} was assumed for the small transistor device as that in the large diode device. This can actually be not true since the incident light intensity in the small transistor device is $3200\times$ stronger than that in the big diode device. As stronger light intensity results in a larger density of carriers, the recombination probability P_{recom} of the photocarriers in germanium could be much greater. According to this JFET transistor with photovoltaic voltage model, to produce channel current of $36.5\mu A$, the effective gate voltage in the Photo-Hetero-JFET is calculated to be $0.012V$ through Eqn.(4-5). Thus the photocurrent in the heterojunction that could have presented this open-circuit voltage is $7.3822\times 10^{-14}A$ (via Eqn.4-4), thereby indicating that this $3200\times$ stronger light intensity results in a recombination probability that is $\sim 16,255$ greater.

Let's apply this model to the transient response of the Photo-Hetero-JFET. According to the expression of JFET channel current (Eqn.4.5), the effective photovoltage on the gate of the Photo-Hetero-JFET that generates a peak channel current of $40.8\mu A$ ($35.6\mu A$ dark current plus $5.2\mu A$ ac peak current) should be $0.069V$. So again through the photovoltaic equation (Eqn.4.4), the photocurrent in the heterojunction of the transistor at this peak is $2.09\times 10^{-12}A$. If we compare this photocurrent value with the peak photocurrent transient response of the heterojunction diode device (Fig.4-19), which is $0.48\mu A$, taking into account the factor of $A_{gate}(0.1\mu m^2)/A_{spot}(50\mu m^2)$, we find that $3200\times$ more intense light incident on the small transistor again causes the recombination probability in germanium to increase, but only by a factor of 459 in this transient case, much smaller than that in the continuous-wave case. One could argue that, this is because the peak power in the laser pulse is already big so a more focused illumination does not have as much effect as when the power to begin with is moderate. Moreover, a photovoltaic $I_{ph}-V_{oc}$ relation established through Eqn.4.4 normally describes the solar cell in steady state and it's questionable whether it can be applied to the transient case. This is because the time scale of the laser pulse ($\sim 4ps$) may be too short for the I-V curve to accurately describe carrier transport across the p-Ge/Si junction.

In conclusion, although the experimental data of Photo-Hetero-JFET, together with that of the heterojunction diode, seem to fit in this "JFET transistor with photovoltaic voltage" model after assuming a factor of increase in recombination probability, there's no evidence from the experiment alone that can prove its validity in the interpretation of Photo-Hetero-JFETs.

II. JFET transistor with trapped charge model

Another model that is proposed for the operation of Photo-Hetero-JFETs is the "JFET transistor with trapped charge" model. In this model, it is the trapped charge in

germanium which attracts electrons into the channel that decreases channel depletion and increases the channel current, i.e.

$$\Delta I_{ch} = qv_{sat}WN_D(-\Delta W_D).$$

If a 100% electro-static coupling efficiency is assumed, the number of electrons n_e that are introduced in the channel is then the same as the number of trapped holes n_h in germanium. And the change in channel depletion is thus

$$\Delta W_D = -\frac{n_h}{A_{gate}N_D}.$$

In our previous discussion on the fall-time of the time resolved response, it is believed that the interaction of photocarriers with traps causes the dispersion of carrier dwell time in germanium and hence the prolonged photoconductivity modulation in the Photo-Hetero-JFET. From the transient response of the heterojunction diode device to the pulsed laser (see Fig.4-25), one can estimate the total number of photocarriers that have a dwell time smaller than 100ns, or, in a simplified “one trap” model, the total number of photocarriers that are once captured in traps of lifetimes shorter than 100ns. By integrating the current pulse within one period of 100ns but excluding the baseline current, the corresponding trapped charge is

$$Q_{trap} = (I_{ave} - I_{baseline}) \cdot \tau_{period} = (0.31\mu A - 0.27\mu A) \times 100ns = 4 \times 10^{-15}C$$

and the corresponding number of trapped holes is

$$n_{trap} = \frac{Q_{trap}}{e} = \frac{4 \times 10^{-15}}{1.6 \times 10^{-19}} = 25,000.$$

Thus there are 25,000 traps in the germanium of the heterojunction diode that have lifetime shorter than 100ns and are involved in capturing photocarriers. The density of these traps is then

$$\frac{n_{trap}}{A_{diode}} = \frac{25,000}{1.6 \times 10^{-3} cm^2} = 1.5625 \times 10^7 cm^{-2}.$$

In the Photo-Hetero-JFETs, when the incident light is more focused and 3200× more intense, it is expected that the density of traps with lifetime shorter than 100ns that are involved in capture of carriers (basically holes) is much larger, and for now, we assume linearity, 3200× larger. Therefore, the number of trapped holes that are to be released within 100ns and hence contributes to the transient peak is

$$1.5625 \times 10^7 cm^{-2} \times 3200 \times A_{gate} (0.1\mu m^2) = 50.$$

Again if the electrostatic coupling efficiency is 100%, 50 electrons are introduced in the channel and the channel depletion is reduced by

$$-\Delta W_D = \frac{n_h}{A_{gate}N_D} = \frac{50}{0.1\mu m^2 \times 4.02 \times 10^{16} cm^{-3}} = 12.43nm.$$

The change in the channel current is thus

$$\begin{aligned}\Delta I_{ch} &= qv_{sat}WN_D(-\Delta W_D) \\ &= 1.6 \times 10^{-19} \times 10^7 \text{ cm} / \text{s} \times 10^{-4} \text{ cm} \times 4.02 \times 10^{16} \text{ cm}^{-3} \times 12.43 \times 10^{-7} = 7.99 \mu\text{A}\end{aligned}$$

which is only slightly larger than the experimentally observed peak of 5μA (Fig.4-26). This slight difference may be attributed to the fact that the density of traps involved in the fast response is not linear with the light intensity. It can be also due to the fact that electrostatic coupling between the trapped charge in the gate and the induced charge in the channel is not 100% as assumed. For a junction-FET with channel length as short as 100nm, some of the electric field lines originating from the gate charge can end in source or/and drain instead of ending in channel leading to a reduced electrostatic coupling.

Following the similar reasoning, in time-resolved response of Photo-Hetero-JFET, the baseline current of 0.2μA indicates that, when equilibrium is reached after the pulsed laser is turned on, there are always two traps ($50 \times 0.2\mu\text{A} / 5\mu\text{A} = 2$) in the germanium gate that are filled; and when the pulsed laser is turned off, these two trapped charges are released, but at a time scale much longer than 100ns.

Similarly, the current on the falling edge at each instant should have been the integral of the transient current in the diode device up to that instant, had the illumination intensity in both cases been the same. However, as pointed out in the previous discussion, the complex dynamics between traps and free carriers is not a simple linear relation with carrier density. That's probably the reason why the supposed integral relation is not seen. In explaining the response of the Photo-Hetero-JFET to continuous-wave laser using the JFET transistor with trapped charge model, 0.9μA current change in the channel suggests that there are 9 trapped photocarriers in the germanium gate in steady-state.

It is found that the response of the Photo-Hetero-JFET in both continuous-wave and pulsed illumination goes linearly with the incident light power (table 4-1 and 4-2). This fits in the model of “JFET transistor with trapped charge” too, since

$$\Delta I_{ch} = qv_{sat}WN_D(-\Delta W_D) = qv_{sat}WN_D \cdot \frac{n_h}{A_{gate} \cdot N_D} = qv_{sat} \cdot \frac{n_h}{L_{gate}},$$

and statistically n_h scales linearly with the incident intensity.

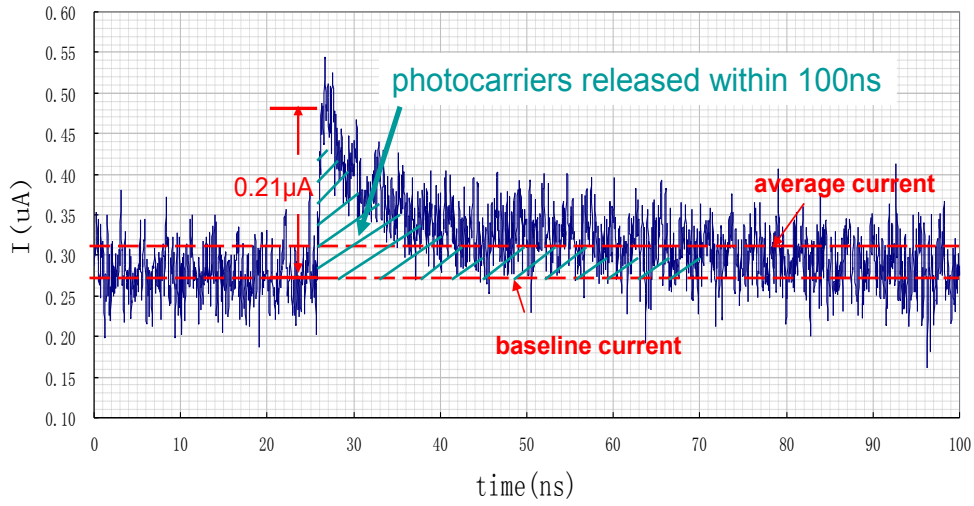


Fig.4-25 Transient photocurrent in the heterojunction diode under pulsed laser

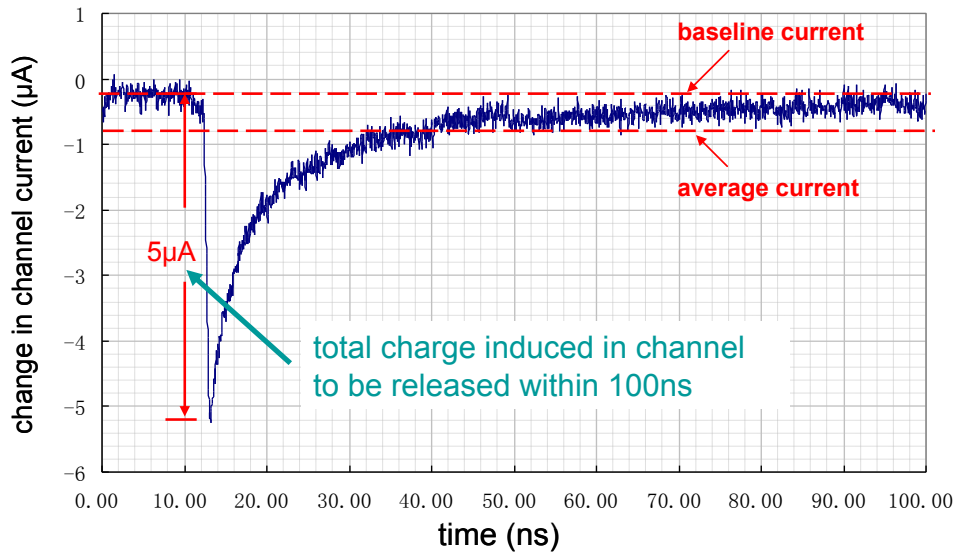


Fig.4-26 Transient current change in the Photo-Hetero-JFET channel under pulsed laser

This model that relies on trapped charges in the gate to electrostatically modulate the JFET channel conductance well explains the experimental results of both Photo-Hetero-JFETs and heterojunction diode devices. The model is actually found to be very similar to the operating mechanism of a *photoconductor* as will be described shortly.

average power of input pulsed laser	peak amplitude of pulsed response on a 50 Ω load
3 mW	3.25 mV
1.5 mW	1.75 mV
0.75 mW	0.9 mV
0.375 mW	0.5 mV
0.188 mW	0.2 mV

Table.4-1 Peak amplitude of pulsed response vs. average power of the pulsed laser

III. Photoconductor model

The performance of the Photo-Hetero-JFET can also be explained in a photoconductor framework, since the gain in Photo-Hetero-JFETs is based on trapped charges and hence is similar to photoconductive gain. In a photoconductor, with photocarrier generation at rate of F and carrier lifetime being τ , at steady-state the number of photocarriers in the photoconductor is then

$$N = F \cdot \tau.$$

So the photocurrent formed in the photoconductor is

$$I = \frac{N}{L} qv = \frac{N}{L} q \frac{L}{T_r} = Fq \frac{\tau}{T_r},$$

in which L is the length of the photoconductor and T_r is the transit time. The photoconductive gain is hence defined as

$$G = \frac{\tau}{T_r}.$$

Now we apply the photoconductor model to analyze the experimental results of the Photo-Hetero-JFET. Under continuous-wave illumination, according to previous estimation based on trapped-charge model, the total number of effective holes in the gate that can attract electrons into the channel in steady state is 9 in total. As $N = F \cdot \tau$, with the carrier generation rate of

$$F = \frac{I_{ph}(\text{from Eqn.4-2})}{e} = \frac{1.2nA}{1.6 \times 10^{-19} C} = 7.5 \times 10^9 / s,$$

the equivalent average carrier lifetime τ in the channel is

$$\tau = \frac{n}{F} = \frac{9}{7.5 \times 10^9 / s} = 1.2ns.$$

So the expected photocurrent in the channel would be

$$I = eF \frac{\tau}{T_r} = 1.6 \times 10^{-19} \times \frac{9}{1ps} = 1.44\mu A.$$

Note that the transit time T_r is 1ps in the 100nm channel with 0.5V drain-to-source bias.

This estimated current is very close to the experimental value of $0.9\mu\text{A}$. Also, the DC photoconductive gain G estimated from the photoconductor model, which is often referred to as “secondary photoconductivity” – to be distinguished from primary responsivity, is

$$G = \frac{\tau}{T_r} = 1200,$$

which is not very different from the experimentally obtained gain of ~ 750 .

The same photoconductor concept can be applied to explain the transient response of the Photo-Hetero-JFET. However, in this time-resolved situation, as there is a distribution of charge dwell-time in the gate, i.e. a distribution of carrier lifetime in the channel, the photoconductive gain accordingly has a gain spectrum. Suppose the number of carriers with lifetime τ_i is N_i , the gain at frequency $f_i = 1/\tau_i$ is

$$G_i(f_i) = \frac{N_i}{\sum_i N_i} \cdot \frac{\tau_i}{T_r}.$$

Based on the tail of transient response of heterojunction device, one can estimate the distribution of photocarriers with dwelling time between $\sim 50\text{ps}$ (the onset of the tail) and 100ns (duration between adjacent laser pulses), and from there, a qualitative profile of photoconductive gain spectrum for the Photo-Hetero-JFET from 10MHz to 20GHz can be obtained. Fig. 4-27 presents this normalized gain spectrum. We see that most gain of the Photo-Hetero-JFET is slow.

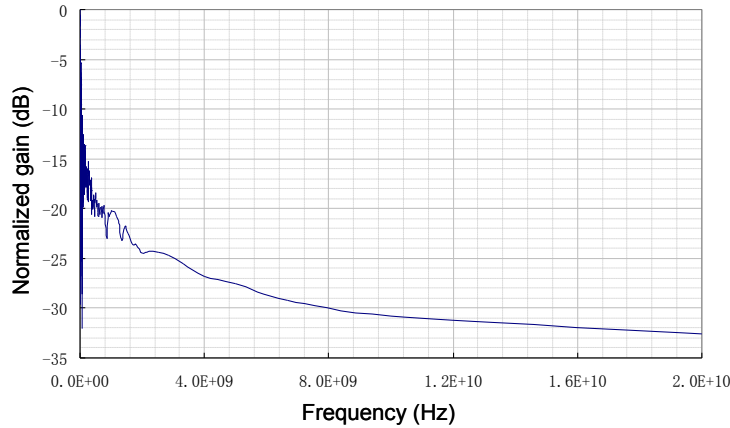


Fig. 4-27 normalized gain spectrum from 10MHz to 20GHz estimated from transient response of heterojunction device.

4.4.2 Dependence of gain frequency spectrum on Ge film quality

In both the JFET model with trapped charges and the photoconductor model, the gain spectrum (gain versus frequency) of the Photo-Hetero-JFETs relies on the “lifetime”

distribution of “traps”, or more physically, the dwell time distribution of photocarriers in germanium. The latter in turn depends on the innate material quality of the germanium film grown. Here in the Photo-Hetero-JFETs built out of the thermally-evaporated germanium that can be as disordered as amorphous, although the DC gain is ~ 750 , most of the photo-gain is too slow for 10GHz or faster applications (see Fig.4-27). Thus, if the germanium film is less disordered, the dispersion of the carrier transit time is expected to be less, and one can expect that more gain goes to the high frequency part of the spectrum. Moreover, as stated earlier, less disordered germanium film would suffer less from geminate recombination leading to greater quantum efficiency.

The three models analyzed above should be compatible with one another – they are connected by the inherent physics behind Photo-Hetero-JFETs but with different interpretations. Of the three, *JFET model with trapped photo-charges* (Model II) best describes the experimental data. The photoconductor model also applies since it is equivalent to Model II in that both depend on trapped charges. So, the gain of Photo-Hetero-JFETs can be described by transconductance gain and/or secondary photoconductivity (photoconductive gain). However, Model I - JFET transistor with photovoltaic voltage, doesn't show strong evidence of fitting the device data. As mentioned above, transient open-circuit voltage under pulsed illumination cannot be simply extracted from the I-V curve. A more proper way to obtain the transient voltage V_G is by counting photo-generated charges Q_{ph} on junction capacitance C_{dep} , i.e. $V_G = Q_{ph}/C_{dep}$. After that, gate voltage V_G can be substituted in Eqn. 4.5 or 4.6 of Model I to obtain the channel current. In fact, such alteration of Model I by using depletion charge in obtaining the gate voltage actually transforms Model I to Model II, which indicates that these two models should indeed be compatible. The difference is simply that, photovoltaic picture is more appropriate for continuous wave situations while the photo-charge method applies to transient cases.

4.4.2 Recap on the influence of germanium film quality

Along different stages of our discussion, we have pointed out how material quality of germanium film affects the performance of Photo-Hetero-JFETs. Firstly, a defective Ge film is more susceptible to Shockley-Read-Hall (SRH) recombination and even geminate recombination, and thereby the photodetector built on such film suffers from poor internal quantum efficiency. Moreover, in Ge films of poor quality, carrier transport deviates from normal diffusion and/or drift and presents dispersive characteristic. The resulted spread in carrier transit time in the Ge gate hence slows the gain in Photo-Hetero-JFETs. The large gain that the Photo-Hetero-JFET adds to the primary responsivity can indeed compensate its pathetic quantum efficiency to an extent, however, owing to dispersive transport, most of the gain falls in the low frequency spectrum. So it seems imperative to use germanium film of decent quality so that the potential advantages of Photo-Hetero-JFET design can be truly exploited. It is worth repeating that

these potential advantages are its great sensitivity (~ 750 CW gain) offered by the transconductance (or photoconductivity) gain and its fast speed (sharp risetime) inherent of its transistor design.

4.5 Conclusions: Why Photo-Hetero-JFET?

This chapter describes the experimental demonstration of the Photo-Hetero-JFET and its performance analysis in detail. The large mesa p-Ge/Si heterojunction diode device is also characterized to provide reference points in analyzing and understanding the nano-gate Photo-Hetero-JFET.

Responsivity measurement under near-infrared continuous-wave illumination was first performed on the heterojunction device. From this measurement, poor internal quantum efficiency which solely depends on germanium film quality was observed. This is attributed to geminate recombination and severe SRH recombination in heavily defected germanium. I-V curves of the heterojunction with and without light were also obtained and the fit to dark I-V curve was made. This is an excellent tool to parameterize the p-Ge/Si junction and is very useful in subsequent modeling of the transistor device.

We then subjected the Photo-Hetero-JFET to the continuous-wave laser at 1550nm and measured the change in channel current. After correcting for the poor internal quantum efficiency in Ge, we found that for every collected photo-electron in the Ge gate, ~ 750 electrons are induced to flow into the channel current. Hence in the Photo-Hetero-JFET, the DC secondary gain added to the primary responsivity is as large as ~ 750 . Time resolved measurement of the Photo-Hetero-JFET under the pulsed laser at 1550nm was also performed and the transient photo-response was recorded. The observed risetime of ~ 50 ps in the transient response is found to be limited by the bandwidth of the SMA cables. The intrinsic risetime of the Photo-Hetero-JFET should be as fast as ~ 1 ps, i.e. transit-time limited.

In our effort to interpret the relatively long tail in the transient response, we looked at the dielectric relaxation time, which is essentially the time it takes for the trapped holes at Ge/Si junction to discharge. The discharging of junction capacitance through forward resistance of a diode is modeled. The estimated discharge time in the heterojunction of the transistor device is on a much longer time scale than what the tail of the transient response suggests. Thus, the process of dielectric relaxation is found only to account for the very slow falling trail after the initial sharp drop of the tail. Then the attempt of explaining the tail led us to also look at the time-resolved response of the heterojunction diode device under the same laser pulses. The presence of similar slow tail in its transient response suggests of dispersive transport of carriers in the germanium film. This dispersive transport of carriers in the Ge gate, described by either statistical hopping or

trapping-and-detrapping via traps, explains the profile of transient response tail of the Photo-Hetero-JFET and is again suggestive of the poor quality of the poly-germanium film grown.

In fitting for the peak amplitude of the transistor transient response, three physical models were proposed and analyzed. The first two models (Model I & II) are based on the operating principle of a JFET. The difference is that, in Model I, light-induced gate voltage is extracted from the photovoltaic relation derived from the I-V curve, and in Model II, trapped charges in the Ge gate causes change in channel depletion. Model II is also equivalent to extracting the light-induced gate voltage by counting trapped photocharges on junction depletion capacitance. We found that Model I is more applicable to steady-state performance of the Photo-Hetero-JFET and it does not fit the experimental data independently without assuming an increased probability of carrier recombination. Model II, the model of JFET transistor with trapped charges, however, not only explains the peak amplitude of transient response of the Photo-Hetero-JFET, but is also compatible with the dispersive transport phenomenon identified earlier. In application of Model II to the Photo-Hetero-JFET, it is found that *only ~50 photo-holes on the gate/channel junction of $0.1\mu\text{m}^2$ can induce channel current of $\sim 5\mu\text{A}$* , and the decay of current in the channel follows that of the trapped charges in the gate. The photoconductor model is then proposed as Model III since it is very similar to Model II in that its gain mechanism is also based on trapped or relatively immobile charges. Sadly, the large gain of the Photo-Hetero-JFET is found to be mostly distributed in slow frequency components of the spectrum, which again put the pathetic germanium film quality under blame. Despite the limitation imposed by the quality of germanium film on its quantum efficiency and bandwidth, from all previous discussions in this chapter, it is still evident that the Photo-Hetero-JFET with channel length of 100nm and junction capacitance of 52aF is capable of demonstrating great sensitivity and fast speed.

The major advantage of the design of Photo-Hetero-JFETs over that of conventional photodetectors is *its great sensitivity resulted from its extremely small device capacitance!* The Photo-Hetero-JFET that we characterized in this thesis work has a gate of area $0.1\mu\text{m}^2$, and thereby a device capacitance of only 52aF! This is already smaller than 1fF, the targeted capacitance that photodetectors should have in chip-level optical links. With this small capacitance, only ~50 photo-holes in the gate are enough to produce channel current of a few μA . That is to say, if the quantum efficiency of germanium is 100%, *only 8aJ light can produce photocurrent of a few μA !* One would argue that, quantum efficiency of 100% seems impossible; however, now that industry has claimed to have the ability to grow good germanium with ~100nm diffusion length, with the Photo-Hetero-JFET integrated onto chips and light coupled through silicon waveguide, a quantum efficiency of 1% should be readily achievable. Hence, *0.8fJ* is all that needed for the Photo-Hetero-JFET with $0.1\mu\text{m}^2$ gate to generate a few μA . Recall that in an

energy-efficient chip-level optical link, the estimated received optical energy per bit is just around 1fJ. So the sensitivity of this Photo-Hetero-JFET design already meets, if not surpasses, the requirement of chip-level optical communication. Furthermore, as there's still plenty of room for Photo-Hetero-JFETs to scale down in keeping up with the state-of-the-art transistor technology, one would expect even greater sensitivity out of Photo-Hetero-JFETs.

It is worth repeating that the scalability of the photodetector alone is not enough to achieve an extraordinarily small device capacitance. Note that the device capacitance here, as pointed in Chapter 1, refers to the detector-plus-transistor capacitance. A p-i-n photodetector can be scaled down to obtain very small capacitance alone, but it has to be interconnected to amplifier transistor(s), so at a system level, device capacitance has to include wire capacitance and gate capacitance of transistor(s), i.e. $C_{total} = C_{detector} + C_{wire} + C_{gate}$ (Fig.4-28). The Photo-Hetero-JFET, however, seamlessly integrates a germanium photodetector with an amplifying transistor, eliminating unnecessary capacitance components. Also, since there's no contact on the germanium gate, it gets rid of more wire capacitance.

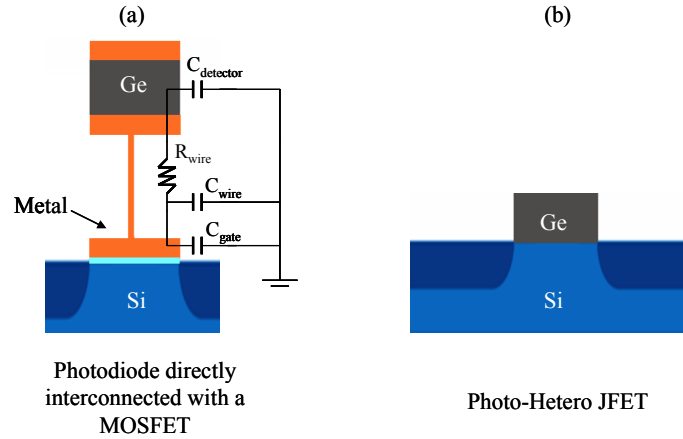


Fig. 4-28 (a) traditional receiver (b) Photo-Hetero-JFET

The sensitivity benefit of Photo-Hetero-JFET that we described above comes from the fact that, owing to extremely small gate capacitance, even with small amount of incident photons the effective gate voltage in the JFET is big enough to produce decent channel current. At this level, the benefit is only revealed within the device itself. However, the significance of small device capacitance can be better appreciated when Photo-Hetero-JFET is integrated in an actual optical communication system.

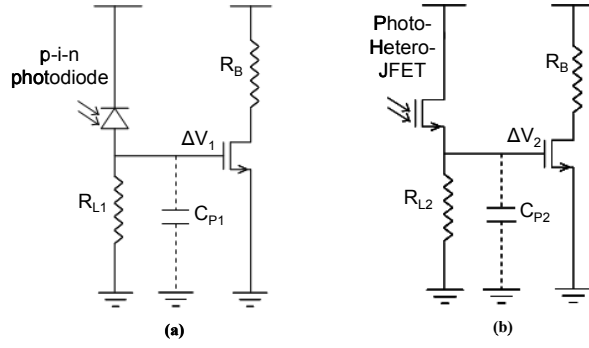


Fig. 4-29 Circuits of simplified configuration of receivers with (a) a standard high speed p-i-n photodiode and (b) Photo-Hetero-JFET.

Now suppose that the Photo-Hetero-JFET and a standard high speed p-i-n photodiode (like the one shown in Fig.4-28) are each to be applied in a high bandwidth transceiver, say at 10GHz. The most basic configuration for the p-i-n photodiode would be that its photocurrent is first sent to a TIA (transimpedance-amplifier) before more amplification stages; whereas for the Photo-Hetero-JFET, the next transistor that its photocurrent is sent to can be a TIA, or directly the next logic stage (Fig. 4-29). Of course the real receiver circuit will be much more complicated, but this simplified configuration in Fig. 4-29 will suffice for the purpose of this discussion. The input resistance of the transistor stage following the photodetector, R_{Li} , is chosen so that $R_{Li} \cdot C_{Pi} = 1/\omega_B$, in which ω_B is the required bandwidth of the receiver. So the voltage generated on the transistor gate is

$$\Delta V_i = I_{photo} R_{Li} = I_{photo} \cdot \frac{1}{\omega_B \cdot C_{Pi}} \approx \frac{I_{photo} \cdot \tau_{pulse}}{C_{Pi}} = \frac{Q_{pulse}}{C_{Pi}}. \quad (4-7)$$

The parasitic capacitance usually includes diode capacitance and wire capacitance, i.e. $C_{p1} = C_{detector} + C_{wire}$. For conventional p-i-n photodiodes, especially those flip-chip bonded to typical transceiver circuits, the length of the wire and that of the active region of the detector easily adds up to $>100\mu m$ [78]. An optimistic estimate for the total parasitic capacitance of the p-i-n diode receiver is then $\sim 10fF$. The capacitance for the Photo-Hetero-JFET, on the other hand, can readily achieve $\sim 10aF$, e.g. with a $100nm \times 100nm \times 100nm$ Photo-Hetero-JFET. Also as there is no wire on the Ge gate, wire capacitance comes only from the connection to the next transistor, which in a highly integrated circuit will be on a length scale similar to the transistor itself. Hence the total parasitic capacitance in the Photo-Hetero-JFET preamp circuit is only a few tens of atto-Farads.

Suppose optical pulses which carry 1000 photons each ($\sim 0.16fJ$) are incident on both photodetectors. In p-i-n diode, all 1000 photons can ideally be collected in each pulse, i.e. $Q_{pulse} = 1000 \times 1.6 \times 10^{-19} = 1.6 \times 10^{-16}C$. In Photo-Hetero-JFET, if 1% quantum efficiency is assumed (which is again readily achievable), ~ 10 out of 1000 photons are

collected by Photo-Hetero-JFET which therefore generates photocurrent of $\sim 1\mu\text{A}$. For ease of comparison, we assume that $\sim 1.6\mu\text{A}$ photocurrent flows during the duration of trapped carrier lifetime $\tau \approx 1/\omega_B$. A safe estimate of the trapped carrier lifetime in Photo-Hetero-JFET for 10GHz application, essentially the fall-time of the response pulse, can be 10ps. Therefore, with Eqn. 4-7, a comparison can be made between p-i-n high speed photodetector and Photo-Hetero-JFET implemented in receivers. With p-i-n photodiode, the voltage generated on the TIA gate is

$$\Delta V_1 = \frac{Q_{pulse}}{C_{p1}} = \frac{1.6 \times 10^{-16}}{10 \text{ fF}} = 0.016 \text{ V};$$

whereas the voltage generated on the gate of the transistor following the Photo-Hetero-JFET is

$$\Delta V_2 = \frac{I_{ph} \cdot \tau}{C_{p1}} = \frac{1.6 \times 10^{-6} \times 10 \text{ ps}}{10 \text{ aF}} = 1.6 \text{ V}.$$

We see that the effect of a 1000 times reduction of parasitic capacitance in receiver with Photo-Hetero-JFET dominates and hence a much bigger voltage (100 \times) can be generated on the transistor that follows the photodetector. Also, this voltage of $\sim 1\text{V}$ is big enough to drive next logic stage, which proves that a Photo-Hetero-JFET can indeed be used in a “receiverless” scheme. It is worth repeating that a “receiverless” scheme can get rid of all amplification stages and thereby significantly reduces power consumption and space occupation in chip-level optical communications. Moreover, with optimized cavity-enhanced configuration described in Chapter 1 (Fig. 1-8), quantum efficiency of the Photo-Hetero-JFET can be further increased and hence this performance improvement in an actual receiver setting of Photo-Hetero-JFET over standard photodetectors is even greater. In a word, thanks to the significantly reduced parasitic capacitance with Photo-Hetero-JFET, very little optical power (~ 10 photons) will be needed on the photodetector to produce voltage large enough ($\sim 1\text{V}$) for receiverless configuration to be realized in chip-scale optical interconnects.

The above discussion quantitatively demonstrates the sensitivity benefits that the tiny capacitance ($\sim 10\text{aF}$) associated with the proposed Photo-Hetero-JFET could bring to the photodetector itself and the receiver end of the optical link it is integrated in. We believe that the crucial role of extraordinarily small device capacitance in improving receiver performance makes the design of this highly integrated and scalable photodetector very favorable. Although the fabricated Photo-Hetero-JFET suffers from poor quantum efficiency and slow gain that were brought about by the poor germanium quality, it still showed large secondary photoresponsivity that stems from its small capacitance advantage. Therefore, with decent germanium film (with diffusion length of $\sim 100\text{nm}$) that is available in the industry, the Photo-Hetero-JFET should be able to demonstrate its potential of great sensitivity and fast speed for the application in chip-level optical

communications.

Other possible types of transistor-based photodetectors that can be built on the same Ge/SOI platform include the configuration of *heterojunction bipolar phototransistors*. Fig.4-30 presents one of the possible bipolar device structures. The emitter/base junction is made out of n-Si/p-Ge heterojunction so that with a wide bandgap emitter, injection of photo-electrons from Ge base back into Si emitter is blocked thereby ensuring a close-to-unity emitter injection efficiency. The thickness of neutral base region is required to be smaller than the minority carrier diffusion length L_D in the base for the bipolar phototransistor to have gain. On the other hand, the neutral base region width cannot be too small so as to prevent the occurrence of punch-through when the space-charge region of emitter-base junction meets that of collector-base junction and the base loses control over collector current.

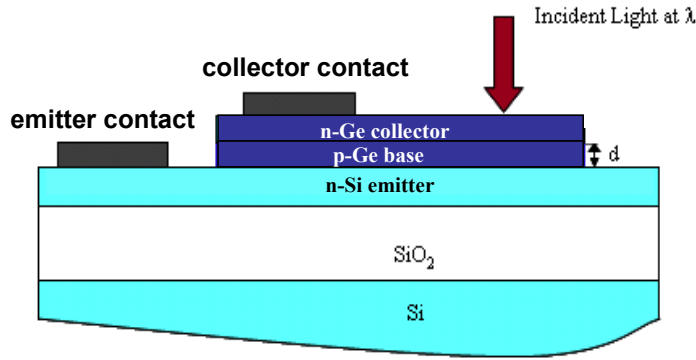


Fig. 4-30 possible structure of heterojunction bipolar phototransistor built on Ge/SOI

However, it is extremely hard to achieve this in the poly-Ge/SOI samples that we had available for making Photo-Hetero-JFETs, since the effective diffusion length estimated for electrons in the poly-Ge is only $\sim 1\text{nm}$, which is unphysically small, and the neutral region of p-type base must be thinner than that for bipolar gain! This is almost impossible since such thin base, even if it could be realized, would be very susceptible to punch-through with varied base bias. Moreover, to counter-dope part of 100nm p^+ -Ge film into n-type and make a shallow junction is also not an easy task to accomplish in our p-Ge/SOI samples. All the n-type dopant ions e.g. Phosphorous and Arsenic diffuse very fast in Germanium; hence it's difficult in controlling dopant diffusion in the annealing step either after ion implantation or after applying spin-on-dopants. For the reasons mentioned above, bipolar phototransistor configuration is indeed infeasible in the p-Ge/SOI material that we have. Nonetheless, given a heterogeneously grown Ge film with decent diffusion length ($\sim 100\text{nm}$) on Si or SOI substrate, the bipolar phototransistor is definitely a good design to go after. The operating mechanism of an HPT is discussed in Chapter 2. Similar to that of a photoconductor, an HPT is capable of producing large

internal gain. A vertical HPT structure also facilitates better base-width control since it is easier to grow films of extremely small thickness than patterning tiny lateral patterns.

Chapter 5 Conclusion

This dissertation shows our dedication to generating a technology of photodetectors for application in chip-level optical communication. The photodetector that this thesis work is focused on is the Ge/SOI Photo-Hetero-JFET. It is based on the structure of silicon junction FET, but the electrical gate is replaced by a photosensitive germanium mesa. So instead of electrical voltage, near-infrared light signals are incident on the electrically-floating gate, and then generate electron-hole pairs there to modulate conductance of the silicon channel underneath. This Ge/SOI Photo-Hetero-JFET is compatible with state-of-the-art CMOS technology and can be easily integrated onto chip with waveguides and other amplifier circuitry. More importantly, the Photo-Hetero-JFET can be monolithically scaled down like a transistor to achieve extremely small device capacitance, which is considered an essential quality for photodetectors in chip-scale optical interconnects.

Chapter 1 of this dissertation gives an introduction to the background and motivation behind the design of Photo-Hetero-JFET. The traditional electrical wires used on chips suffer from severe power consumption, latency and many other problems, and thus increasingly becomes the bottleneck that limits the performance of signal processing systems. On the other hand, the advantages of optics, including low loss, its quantum mechanical nature and so on, make optical interconnects a most promising candidate for replacing electrical wires. The major technological challenge that the chip-scale optical interconnect then faces is to achieve one order of magnitude lower energy consumption than the state-of-the-art electrical interconnect, i.e. 100fJ/bit. This in turn requires the energy consumed at receiving end be less than 1fJ/bit. Such stringent requirement can only be possibly achieved by photodetectors that are *highly-integrated with extremely small device capacitance*. Various types of photodetectors are reviewed in Chapter 1 while they are gauged against the above-mentioned criterion. Phototransistors, in particular, can be readily integratable and scalable to obtain extraordinarily small capacitance, and their internal gain mechanism can further enhance photosensitivity. With that, the subject of this thesis work, Ge/Si Photo-Hetero-JFETs, is proposed at the end of Chapter 1.

Chapter 2 starts from the fundamentals of the Ge/Si heterojunction itself, which is the core of Photo-Hetero-JFETs where most interesting physics happen. The challenge in heterogeneous growth of germanium on silicon comes from the 4% lattice mismatch between the two. Various approaches to address this are presented in the chapter. It then looks at photocarrier generation, transport and separation in the heterojunction. The separation of photocarriers is facilitated by type II band-alignment of p^+ -Ge/n-Si junction and in effect induces a photovoltage across the junction; while the carrier transport is

limited by diffusion in germanium since all the space charge region of the junction all falls on the silicon side. The quantum efficiency of $p^+-\text{Ge}/n\text{-Si}$ heterojunction in response to light is hence limited by the electron diffusion length L_D in germanium. However in very defective germanium film, the model of photocarrier diffusion itself is not appropriate. Geminate recombination happens even before Shockley-Read-Hall recombination. This severely reduces the percentage of photocarriers that can be collected in the heterojunction and deteriorates quantum efficiency of the photodetector further. The physics of the Ge/Si heterojunction helps in understanding the Ge/SOI Photo-Hetero-JFET design. The operating mechanism of Ge/SOI Photo-Hetero-JFETs can be described either as a silicon junction FET modulated by the induced photovoltage on Ge/Si junction, or a photoconductor whose conductivity is enhanced by trapped photo-holes at Ge/Si junction interface.

Device fabrication is discussed in Chapter 3. Ge/Si Photo-Hetero-JFETs with submicron germanium gate ($100\text{nm} \times 1\mu\text{m}$) are the main devices that are fabricated for this dissertation work. Simple junction photodiodes are also fabricated out of the same Ge/SOI material stack as reference devices for characterization and interpretation of the heterojunction. The starting material stack consists of thermally evaporated poly-germanium film and SOI substrate that the germanium film is grown on. Chapter 3 also briefly described the fabrication process of large area ($400\mu\text{m} \times 400\mu\text{m}$) photodiode devices, but devotes most of its efforts into an in-length discussion on fabrication of Ge/Si Photo-Hetero-JFETs. The challenges in fabricating Photo-Hetero-JFETs include counter-doping the silicon substrate without an extra ion implantation step, activating dopants without melting Ge gate and etc. Those challenges are solved by innovative approaches which are presented in Chapter 3. For example, taking advantage of lateral straggle which is normally considered detrimental in ion implantation, together with the ion diffusion during post-annealing process, we indirectly “doped” the silicon channel underneath the 100nm germanium gate from p^- to n -type.

Experimental demonstration and performance analysis of Ge/Si Photo-Hetero-JFETs are the main focus of this dissertation work, and are discussed in great detail in Chapter 4. In order to provide references in analyzing and understanding the nano-gate Photo-Hetero-JFET, large mesa $p\text{-Ge}/\text{Si}$ heterojunction diode device is also characterized. Responsivity measurement performed on the diodes under CW illumination reveals that quantum efficiency of the Ge/Si heterojunction in response to NIR light is very poor. The diffusion length estimated for electrons in germanium is unphysically small indicating that photocarriers possibly suffer geminate recombination in addition to severe SRH recombination, and that the thermally evaporated germanium is indeed heavily defected. The I-V curves of the heterojunction are also obtained from the responsivity measurement to be an excellent tool to parameterize the junction for modeling of the transistor device.

The Photo-Hetero-JFET is firstly characterized under continuous-wave laser at 1550nm and the change in channel current is measured. The absolute responsivity is poor, i.e. 3×10^{-4} ; however, if one takes into consideration the extremely poor internal quantum efficiency caused by the low quality germanium film, one would find that every one of collected photons that have produced electron-hole pairs that survived recombination in germanium (geminate and SRH recombination) could lead to generation of ~ 750 electrons in the silicon channel. This indicates a DC secondary photon-gain of 750 on top of the primary responsivity! In order to evaluate Photo-Hetero-JFETs in high-speed applications, time-resolved measurement of the photodetector under pulsed laser at 1550nm was performed and transient photo-response was obtained. The photoresponse pulse shows sharp risetime of ~ 50 ps, which is thought to be limited by the bandwidth of SMA cables. If the same Photo-Hetero-JFET is fully-integrated in an on-chip receiver system with state-of-the-art amplifier circuitry, it should be able to present its intrinsic risetime, which is transit-time limited, of ~ 1 ps. However, the long fall-time of the transient photo-pulse (~ 26 ns) is a big issue in the Photo-Hetero-JFET. Initially the long tail was attributed to dielectric relaxation time, which is essentially the time it takes for trapped photo-holes at Ge/Si junction to discharge. By examining the transient response of p-Ge/Si heterojunction diode device which also shows a similar tail, we found that dielectric relaxation is not the main mechanism, as it should occur at much longer time scale and therefore cannot account for the initial sharp drop in the tail. Instead, the transient tail of the diode device suggests the presence of dispersive transport of photocarriers in germanium. This anomalous transport of carriers is described by either statistical hopping or trapping-and-detrapping via traps, and it explains the signature profiles of transient tails of both Photo-Hetero-JFET and p-Ge/Si heterojunction diode device. Furthermore, since dispersive transport only happens in amorphous or very defective material, its presence in the germanium gate again indicates the poor quality of the film.

Three physical models are proposed as operating mechanisms of Photo-Hetero-JFET in an attempt to fit for the peak amplitude of transient response. The first one models the photodetector as a Junction FET and it extracts the light-induced gate voltage from the photovoltaic relation derived from I-V curve. It is named in this thesis work as **JFET with photovoltaic voltage model**. This model is found to be more applicable to describing steady-state performance of the device. By assuming an increased probability of carrier recombination in the much smaller transistor device under much denser illumination, as compared to larger diode device under weaker illumination, this model can explain the amplitude of continuous-wave photoresponse of Photo-Hetero-JFET. Although similar assumptions could be made in the case of pulsed illumination to explain the peak amplitude of transient response, it is believed that the model is not appropriate here, because the time scale of the laser pulse (~ 4 ps) may be too short for the I-V curve

to accurately describe carrier transport across the p-Ge/Si junction.

The second model is also based on the operating principle of a JFET, but its difference from the first model is that it attributes the modulation of channel conductance to trapped charges in the Ge gate. This model is named here as **JFET with trapped charge model**. It is also equivalent to extracting light-induced gate voltage by counting trapped photocharges on junction depletion capacitance. The second model well explains the peak amplitude of device transient response. It is also found to be compatible with the dispersive transport phenomenon, i.e. trapping-and-detrapping of photocarriers, since the decay of transient tail follows that of trapped charges in the gate. With this model, the design of the Photo-Hetero-JFET is proven to possess great sensitivity in that *only ~50 photo-holes on the gate/channel junction of $0.1\mu\text{m}^2$ can induce channel current of $\sim 5\mu\text{A}$!* The **photoconductor model** is proposed following the second model since its gain mechanism is also based on trapped charges. Although the secondary photoconductivity or photo-transconductive gain of Photo-Hetero-JFET is large, most of it unfortunately falls in low frequency components of the spectrum. This again is due to the dispersive nature of carrier transport, which in turn results from poor germanium film quality.

One attribute of the Photo-Hetero-JFET design that makes the device highly sensitive is its extraordinarily small device capacitance ($\sim 52\text{aF}$). This is achieved by scaling down the gate of the phototransistor to a submicron size ($100\text{nm} \times 1\mu\text{m}$). Another attribute of the Photo-Hetero-JFET is that it seamlessly integrates the germanium photodetector with a transistor that further adds gain. This design eliminates the need of following amplification stages when the device is actually used in a transceiver, i.e. a “receiverless” photodetection scheme. While the advantages of these attributes are already prominent at the device level, they are even better appreciated in the context of an actual optical communication system. A “receiverless” scheme can significantly reduce parasitic capacitance of the transceiver; together with extremely small device capacitance, the total system capacitance can be indeed as low as $\sim 1\text{fF}$ (or even a few tens of aF). It can be quantitatively proven that, with an internal quantum efficiency of 10% readily achievable in decent germanium film, very little optical power (~ 100 photons) will be needed on the Photo-Hetero-JFET to produce voltage large enough ($\sim 1\text{V}$) for receiverless configuration to be achieved in chip-level links.

This dissertation work proposed and realized the design of a CMOS-compatible and potentially very sensitive photodetector, the Ge/SOI Photo-Hetero-JFET. Its extremely small device capacitance as well as its seamless integration with silicon circuitry makes the design of Photo-Hetero-JFET highly favorable in the development of chip-level optical interconnect system. Currently, the fabricated Photo-Hetero-JFETs suffer from poor quantum efficiency and slow gain which were brought about by the poor germanium quality. Nonetheless, the device still presents impressive secondary photoresponsivity

and great potential in its bandwidth improvement. It is believed that with decent germanium films (with diffusion length of $\sim 100\text{nm}$) that are already available in the industry, the Photo-Hetero-JFET is capable of demonstrating great sensitivity and fast speed in the application of chip-level optical communications.

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