The Piezoelectric Transformer Field Effect Transistor

Sapan Agarwal and Eli Yablonovitch

University of California, Berkeley, 550 Sutardja Dai Hall, Berkeley, CA 94720

Email: sapan@berkeley.edu, Phone: 510-664-4469

In order to reduce the power consumption of modern electronics, the operating voltage needs to be significantly reduced. Unfortunately, conventional transistors fundamentally require around half a volt to switch. On the other hand, electrical wires only need millivolts to overcome noise and communicate information. This voltage mismatch results in a significant amount of power being wasted by charging the wires to a high voltage. To overcome this mismatch, either a new low voltage switch[1-4] or a voltage transformer is needed. In this paper we propose a new CMOS compatible piezoelectric voltage transformer that can be placed on the gate of each transistor to reduce the voltage needed for switching. This allows for a low voltage to be used to charge the wires while increasing the voltage at the transistor where it's needed. This results in the Piezoelectric Transformer Field Effect Transistor, or PT-FET.

A nanoscale piezoelectric voltage transformer is illustrated in Fig 1(c). When a voltage is applied to the top piezoelectric it expands, squeezing the lower piezoelectric and inducing a polarization charge. The polarization charge creates an electric field which causes a higher voltage at the gate oxide.

In Fig. 2, we show a simulated piezoelectric voltage transformer that results in a 3.4X voltage enhancement! The top piezoelectric is $0.67Pb(Mg_{1/3}Nb_{2/3})O_3–0.33PbTiO_3$ (PMN-PT[5]) and the bottom piezoelectric is PZT-7A (Lead zirconate titanate). The large 10:1 aspect ratio is required to allow the piezoelectrics to expand/contract in the lateral dimension. The electric potential and mechanical strain are simulated using the finite element method in COMSOL multiphysics, using bulk material parameters.

We can further improve the voltage enhancement by charging a series of piezoelectric layers in parallel and then mechanically connecting them in series with the bottom layer as shown in Fig. 3. By polling each of the top layers in alternating directions, all of the layers will expand when a voltage is applied to them. Consequently, each layer will add to the pressure on the bottom layer. This gives a voltage enhancement of 8.2X. If the aspect ratio of the transformer is increased to 20:1 (five 10 nm top layers and a 350 nm bottom layer), a voltage enhancement of 10X can be achieved! This would correspond to a 100X reduction in power used to charge the wires ($P=CV^2$).

In Fig. 4 we show simulated results of what happens if the gate capacitance, top piezoelectric thickness and bottom piezoelectric thickness are changed. As shown in Fig. 4(a), the voltage amplification drops to 1 if the gate capacitance is too high. This is because the piezoelectric cannot provide enough charge if the capacitance is too high. In a scaled transistor a channel carrier density of around $10^{12}/cm^2$ will be needed in the on state to maintain a high channel conductance. At half a volt in a 20 nm channel this corresponds to an effective capacitance of $C=Q/V= 64$ aF/μm. As seen from Figure 4(a) this corresponds to a voltage amplification around 3X. In Fig. 4(b) and 4(c) we show the voltage amplification vs the top piezoelectric thickness and vs the bottom piezoelectric thickness respectively. When the top piezoelectric is too thin, it is mechanically clamped (it cannot shrink laterally while expanding vertically to preserve volume) and so the amplification decreases. If the top piezoelectric is too thick or the bottom piezoelectric is too thin the mechanical energy will be wasted in squeezing the top piezoelectric rather than the bottom one, resulting in a lower voltage amplification.

Next, we estimate the mechanical speed. Since this device involves physical motion, the speed will be limited by the rate at which the piezoelectrics can expand/contract. We estimate this by dividing the speed of sound (~3000 m/s) by the height of the piezoelectric stack (200 nm) to get a maximum speed of 15 GHz.

We have proposed a new piezoelectric voltage transformer that can be used to significantly reduce the voltage of modern electronics. A two layer piezoelectric stack can increase the voltage by 3.4X and a 6 layer stack can amplify the voltage by 8.2X. Increasing the transformer aspect ratio and increasing the number of layers can allow for arbitrarily high voltage amplification. A scaled piezoelectric transformer has a reasonable mechanical speed of 15 GHz and promises to significantly reduce the power required for electronic communications.

Acknowledgment: This work was supported by the Center for Energy Efficient Electronics Science (NSF Award 0939514). We would like to thank Sayeef Salahuddin for helpful discussions.

[1] D. E. Nikonov and I. A. Young, IEEE Electron Devices Meeting (IEDM), 2012, pp. 25.4
[2] S. Salahuddin and S. Datta, Nano Letters, vol. 8, pp. 405-410, 2008/02/01 2007.
[3] D. Newns, B. Elmegreen, X. Hu Liu, and G. Martyna, Journal of Applied Physics, vol. 111, p. 084509 2012.
[4] T. N. Theis and P. M. Solomon, Proceedings of the IEEE, vol. 98, pp. 2005-2014, 2010.
[5] R. Zhang, B. Jiang, and W. Cao, Journal of Applied Physics, vol. 90, pp. 3471-3475, 2001.

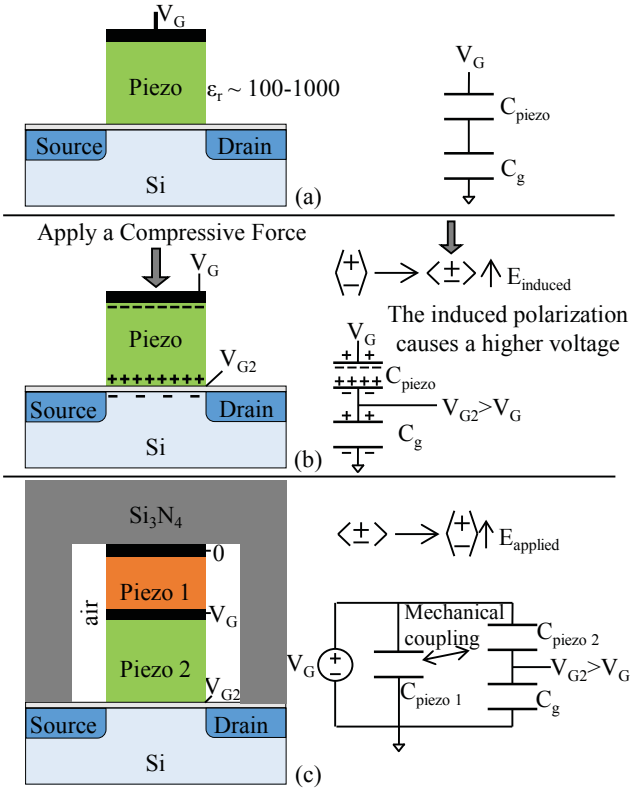

Fig. 1: The operation of a piezoelectric transformer is illustrated (a) A single piezoelectric layer just acts like a series capacitor. (b) Applying a force to the piezoelectric induces a polarization charge and thus electric field which causes $V_{G2}>V_G$. (c) The required force is provided by a second piezoelectric stacked on top of the first piezoelectric.

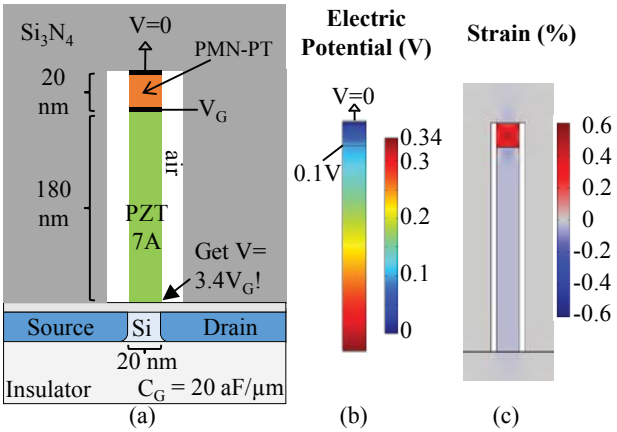

Fig. 2: (a) This structure is simulated in COMSOL and gives a 3.4X voltage enhancement. (b) The electric potential in the piezoelectrics is plotted. The potential scales linearly with V_G and so the enhancement is always 3.4X regardless of V_G. (c) The strain, ε_{zz}, in the structure is plotted. The voltage across the top piezoelectric causes it to expand and compress the lower piezoelectric. The strain is proportional to V_G and is shown for V_G=0.1 V.

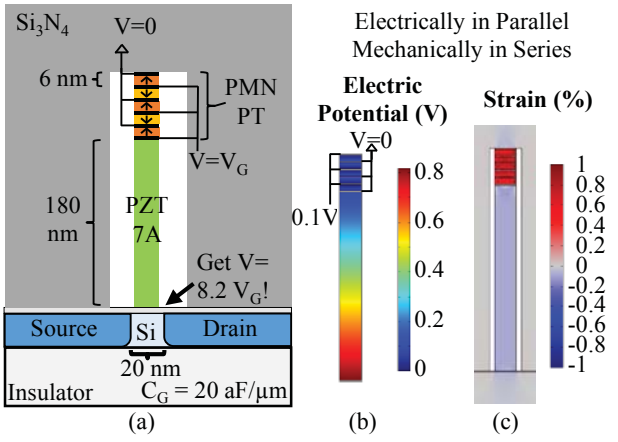

Fig. 3: (a) Multiple oppositely polled piezoelectric layers can be used to increase the pressure on the bottom piezoelectric and thus increase the voltage enhancement. (b) The electric potential in the piezoelectrics is plotted. A 8.2X voltage enhancement is simulated. (c) The strain ε_{zz} in the structure is plotted.

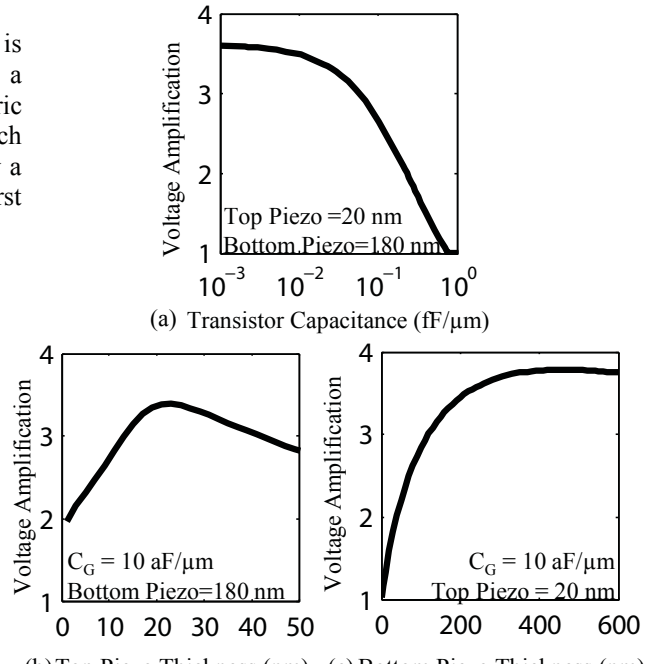

Fig. 4: The voltage amplification vs (a) transistor gate capacitance, (b) top piezoelectric thickness and (c) bottom piezoelectric thickness is shown.