

Band-Edge Steepness Obtained From Esaki/Backward Diode Current–Voltage Characteristics

Sapan Agarwal, *Member, IEEE*, and Eli Yablonovitch, *Fellow, IEEE*

Abstract—While science has good knowledge of semiconductor bandgaps, there is not much information regarding the steepness of the band edges. We find that a plot of absolute conductance, I/V versus voltage V , in an Esaki diode or a backward diode will reveal a best limit for the band tails, defined by the tunneling joint density of states of the two band edges. This joint density of states will give information about the prospective subthreshold swing voltage that could be expected in a tunneling field-effect transistor. To date, published current–voltage characteristics indicate that the joint band-tail density of states is not steep enough to achieve <60 mV/decade. Heavy doping inhomogeneity, among other inhomogeneities, results in a gradual density of states extending into the bandgap. The steepest measured tunnel diodes have a tunneling joint density of states >90 mV/decade.

Index Terms—Backward diode, band tails, density of states, Esaki diode, subthreshold swing, tunneling, tunneling field-effect transistor (TFET), Urbach tail.

I. INTRODUCTION

WHILE science has good knowledge on the magnitude of semiconductor bandgaps, there is not much information regarding the sharpness of the band edges. There is great interest in finding a band-edge steepness in the joint conduction/valence band density of states, sharper than the thermal Boltzmann limited value, 60 meV/decade. This is important for designing a steep tunneling field-effect transistor (TFET) [1] as well as a better backward diode [2]. Measurements of the optical Urbach tail (the rate at which optical absorption falls off for photon energies below the bandgap), indicate a joint density of states of 23 meV/decade for Si [3] and 17 mV/decade for GaAs [4]. This seems somewhat promising but the results need to be validated by electrical transport measurements. Ideally, TFETs, Esaki diodes, and backward diodes have current–voltage (I – V) characteristics that are controlled by the band edges, abruptly turning ON when the conduction band on the n-side aligns with the valence band on the p-side of a tunneling junction [5], sometimes called the band-edge energy filtering mechanism. In actuality, the band edge is not perfectly sharp and there are states

that extend into the bandgap, affecting the I – V characteristics of TFETs, Esaki diodes, and backward diodes [6]. We analyze these I – V measurements to infer the joint conduction/valence band density of states. Electrically measured joint density of states have generally indicated a steepness >90 meV/decade, unlike the optical Urbach measurements that are <60 meV/decade in good semiconductors. We attribute this smearing to the spatial inhomogeneity, such as thickness fluctuations, poor interfaces, inhomogeneous electrostatics, and doping inhomogeneity that appears in real devices. That same finite density of states will limit the subthreshold swing voltage of a TFET. Fortunately, these effects can possibly be eliminated or ameliorated.

In intrinsic GaAs, the optical absorption falls off at a semilog rate of 17 meV/decade [4]. Doping the GaAs causes the absorption to fall off more gradually. When doped to $p \sim 10^{20}/\text{cm}^3$, the absorption falls off at a semilog rate >60 meV/decade [7]. This means that if a TFET is heavily doped, it will never be able to use the density of states energy filtering mechanism to achieve a subthreshold swing voltage <60 mV/decade. To interpret electrical transport measurements, we show that the absolute conductance, I/V versus bias voltage V , is proportional to the tunneling joint density of states in Section II. The tunneling joint density of states is the product the joint conduction/valence band density of states and the tunneling transmission probability. This means that two terminal I – V measurements can be used to determine the steepness of the band edge.

Consequently, we can learn how steep a TFET could be without ever building the full TFET. In Section III, we analyze a variety of data from the literature to see what experimental band-edge steepness has been achieved. Finally, in Section IV, we show how this method can be applied to TFETs.

II. INFORMATION FROM ABSOLUTE CONDUCTANCE

As an example, we consider the I – V characteristics of two InAs mesa homojunction Esaki diodes that were grown by Molecular Beam Epitaxy (MBE) [8]. The semilog I – V curves are plotted in Fig. 1(a) and the absolute conductance (I/V) in Fig. 1(b). The $\log\{\text{absolute conductance}\}$ varies smoothly at $V = 0$, offering the prospect for a physical interpretation in terms of fundamental semiconductor properties. Contrariwise, in Fig. 1(a), the semilog plot, $\log\{\text{current}\}$ versus V , diverges at $V = 0$, preventing direct interpretation. Likewise, a plot of $\log\{\text{differential conductance}\}$ diverges on a semilog plot at the Esaki peak,

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The authors are with the University of California at Berkeley, Berkeley, CA 94720 USA (e-mail: sapan@berkeley.edu; eliy@eecs.berkeley.edu).

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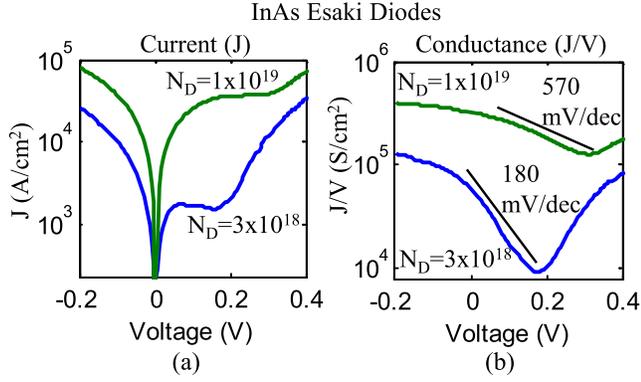


Fig. 1. (a) I - V curves for two InAs Esaki diodes are plotted [8]. The diode was formed through MBE growth and mesa isolation. The p-side doping is $1.8 \times 10^{19}/\text{cm}^3$. At $V = 0$, $\log\{\text{current}\}$ diverges and so the logarithmic slope is meaningless. (b) Alternatively, $\log\{\text{absolute conductance}\}$ passes smoothly through the origin. Increasing the doping results in a significant worsening of semilog conductance swing voltage in mV/decade.

preventing direct physical interpretation. Thus, a $\log\{\text{current}\}$ or a $\log\{\text{differential conductance}\}$ plot does not give us the information we want. By contrast, in Fig. 1(b), the $\log\{\text{absolute conductance}\}$, $\log\{I/V\}$, smoothly decreases from reverse bias, through the origin, and all the way to the forward Esaki region. Consequently, we can interpret the number of millivolts required to get a decade change in conductance. We will now show that the smoothly varying absolute conductance measures the tunneling joint density of states.

We consider the following model for the tunneling current:

$$I \propto \int (f_c - f_v) \times \mathcal{T} \times D_J(E) \times \partial E. \quad (1)$$

The difference between the Fermi occupation probabilities on the p and n sides is $(f_c - f_v)$. \mathcal{T} is the tunneling probability across the junction and $D_J(E)$ is the joint density of states between the valence band on the p-side and the conduction band on the n-side. We are interested in measuring the tunneling joint density of states $\mathcal{T} \times D_J(E)$ in the integrand of (1). The different components of the current integral are shown in Fig. 2(c)–(f), for different bias points. The decreasing tunneling probability is shown in Fig. 2(c). The joint density of states, $D_J(E)$, is shown in Fig. 2(d)–(f). The joint density of states is the product of the band tail in the conduction band density of states, $D_C(E)$, and the band tail in the valence band density of states, $D_V(E)$, as shown in Fig. 2(d)–(f). Going from bias points I–III, the joint density of states exponentially increases. To measure $\mathcal{T} \times D_J(E)$, we need to divide out the effect of the Fermi functions, $f_c - f_v$. Since the area under the curve $f_c - f_v$ is proportional to the applied voltage, dividing by the voltage approximately eliminates its effect.

We quantitatively see this by multiplying and dividing (1) by the integral of the Fermi levels

$$I \propto \int (f_c - f_v) \times \partial E \times \frac{\int (f_c - f_v) \times \mathcal{T} \times D_J(E) \times \partial E}{\int (f_c - f_v) \times \partial E} \quad (2a)$$

$$= qV \times \frac{\int (f_c - f_v) \times \mathcal{T} \times D_J(E) \times \partial E}{\int (f_c - f_v) \times \partial E}. \quad (2b)$$

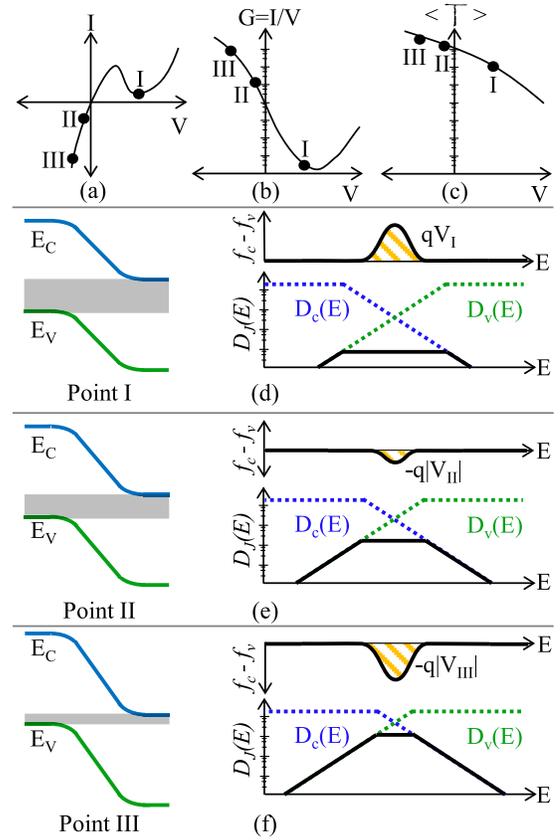


Fig. 2. (a) The I - V curve and (b) conductance for an Esaki diode is plotted. (c) The tunneling probability at different biases is shown. The band diagram, Fermi occupation difference and joint density of states are plotted for bias points (d) I, (e) II and (f) III. (For simplicity, we show conduction, $D_C(E)$, and valence, $D_V(E)$, band edges with equally sloping band tails.) Even though the band edges do not overlap, the band tails still overlap, resulting in a finite joint density of states. The joint density of states exponentially increases when shifting the bias from point I to III and is proportional to absolute I/V . To show this, we need to divide out the effect of the Fermi functions, $f_c - f_v$ from the current. Since the area under the curve $f_c - f_v$ is proportional to the voltage, dividing by the voltage eliminates its effect, approximately, I/V in (b) decreases exponentially at forward bias as the joint density of states decreases its overlap and the tunneling probability decreases.

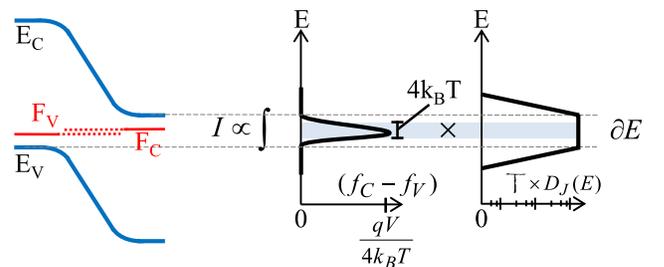


Fig. 3. Current integral (1)–(3) is graphically illustrated. (The Fermi functions and joint density of states on the right, are rotated 90° from Fig. 2.) The integral is essentially given by an average of $\mathcal{T} \times D_J(E)$ over an energy range of $4k_B T$, as indicated by the shaded region.

The second term looks like a weighted average of $\mathcal{T} \times D_J(E)$ over the Fermi functions

$$I \propto qV \times \langle \mathcal{T} \times D_J(E) \rangle. \quad (3)$$

This is shown in Fig. 3.

In our method, we pay little attention to the shape of the Fermi functions. As observed in Fig. 4(a), the ratio

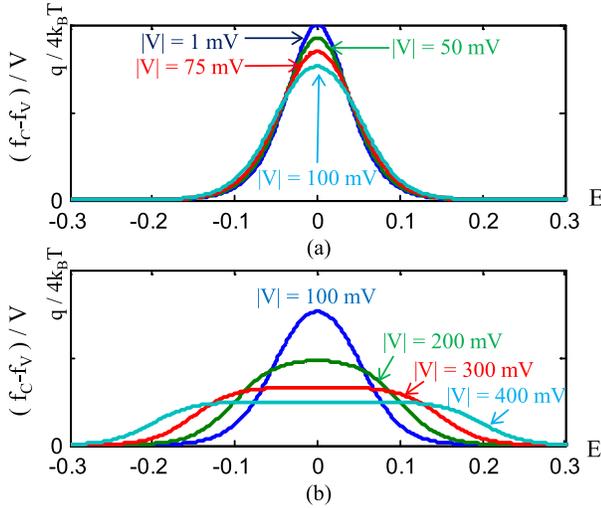


Fig. 4. Normalized Fermi occupation probability, $(f_C - f_V)/V$, is plotted at $T = 300$ K. This illustrates the energy range over which $T \times D_J(E)$ is averaged. (a) For small biases $< 4k_B T/q$ the shape barely changes and so the change in I/V is only due to the change in $T \times D_J(E)$. (b) At larger biases, the Fermi function width starts to increase and is given by V . $T \times D_J(E)$ is changing exponentially while $(f_C - f_V)/V$ is changing linearly. Therefore, I/V still primarily gives the change in $T \times D_J(E)$.

$(f_C - f_V)/V$ barely changes for $V < 4k_B T$. This means that in this range, any change in I/V is due mainly to the change in $T \times D_J(E)$. Consequently, measuring I/V will give us exactly what we are interested in $T \times D_J(E)$. Fig. 4(b) shows $(f_C - f_V)/V$ starts to broaden and the height decreases for $V > 4k_B T$, but even at $V = 400$ mV there is at most a $4\times$ correction, which can safely be neglected with respect to the exponential changes shown in Fig. 2.

The steepness of the tunneling joint density of states in mV/decade is given by

$$S_{T \times D(E)} \equiv \left[\frac{d \log \langle T \times D_J(E) \rangle}{dV} \right]^{-1} \approx \left[\frac{d \log (I/V)}{dV} \right]^{-1}. \quad (4)$$

This is called the semilog conductance swing voltage. Measuring the number of millivolts required to get a decade change in conductance, gives the steepness of $T \times D_J(E)$ and thus the tunneling junction.

A. Interpreting the Tunneling Joint Density of States

The voltage dependence of $T \times D_J(E)$ can be dominated by either the tunneling probability, T , or the joint density of states, $D_J(E)$. Toward forward bias, both the tunneling probability and the density of states will decrease to turn off the tunneling.

Whether T or $D_J(E)$, is the most dominant influence on current will depend on the particular geometry and current level. We distinguish the effects of the T and $D_J(E)$ by approximating: $\langle T \times D_J(E) \rangle \approx \langle T \rangle \times \langle D_J(E) \rangle$ [9]. Evaluating (4), the semilog conductance swing voltage, $S_{T \times D(E)}$, gives the sum of the logarithms

$$\left[\frac{d \log (I/V)}{dV} \right]^{-1} = \left[\frac{d (\log \langle T \rangle + \log \langle D_J(E) \rangle)}{dV} \right]^{-1} \quad (5a)$$

$$\left[\frac{d \log (I/V)}{dV} \right]^{-1} = S_{T \times D(E)} = \left[\frac{1}{S_{\text{tunnel}}} + \frac{1}{S_{\text{DOS}}} \right]^{-1} \quad (5b)$$

S_{DOS} measures the steepness of the joint band edge density of states in mV/decade: $S_{\text{DOS}} \equiv [d \log \langle D_J(E) \rangle / dV]^{-1}$. As observed from Fig. 2(d)–(f), the energy averaged joint density of states changes exponentially with bias. S_{DOS} measures the joint density of states steepness, which is the band tail steepness. S_{tunnel} is the semilog slope measuring how steeply the tunneling conductance prefactor changes with respect to bias: $S_{\text{tunnel}} = [d \log \langle T \rangle / dV]^{-1}$. Using the Wentzel-Krammer-Brillouin exponential [10] to evaluate S_{tunnel} for a typical p-n junction gives [11], [12]

$$S_{\text{tunnel}} \equiv \left(\frac{d \log \langle T \rangle}{dV} \right)^{-1} = \frac{2V}{|\log \langle T \rangle|}. \quad (6)$$

With both mechanisms present in any specific case, the observed $S_{T \times D(E)}$ will be steeper than with one mechanism alone, and consequently places a lower limit, $S_{\text{DOS}} > S_{T \times D(E)}$ and $S_{\text{tunnel}} > S_{T \times D(E)}$. At high-current density, T is close to 1, and $|\log \langle T \rangle|$ is small, leading to an undesirably large S_{tunnel} . Achieving a high steepness will then depend entirely on S_{DOS} .

Unfortunately, we observe that the experimental data is actually not very steep at all, calling into question the common optimistic predictions [1], [13], based on a perfectly steep band edge. The key point is that S_{DOS} , which is undoubtedly important at high-current density, is even worse than the measurements, $S_{\text{DOS}} > S_{T \times D(E)}$. Therefore, experimentally observed band-edge steepness is inadequate for the goal of a steep device at high current, irrespective of tunnel thickness modulation, which sometimes performs well at low-current density.

III. ANALYZING PUBLISHED DATA

In this section, we analyze the absolute conductance of several different published tunnel diodes to determine the band-tail steepness. In Fig. 1, we show the current and conductance for an InAs homojunction diode at two different doping levels [8]. Since the conductance is proportional to tunneling joint density of states, we can measure the inverse of the semilog slope of the conductance, $S_{T \times D(E)}$, to find the steepness of the tunneling joint density of states in mV/decade. This is indicated by the inverse slope of the diagonal lines in Fig. 1(b). When the n-side doping is increased from $3 \times 10^{18}/\text{cm}^3$ to $1 \times 10^{19}/\text{cm}^3$, $S_{T \times D(E)}$ drastically increases from 180 mV/decade to 570 mV/decade. This clearly illustrates the dangers of smearing a band edge by doping too heavily.¹

In Fig. 5, we show the current and absolute conductance for a series of mesa GaAs homojunction diodes that were grown by MBE [8]. The n-side doping is $3 \times 10^{19}/\text{cm}^3$ and the p-side doping varies from $N_A = 5 \times 10^{18}/\text{cm}^3$ to $5 \times 10^{19}/\text{cm}^3$. As the doping, N_A , is changed, the absolute conductance changes by three orders of magnitude because the tunneling barrier thickness/depletion region thickness is changing. Nonetheless, the semilog conductance swing voltage only changes from 130 to 165 mV/decade. This small change

¹Contact resistance might present problems at the highest conductance. If we assume the peak conductance is limited by the contacts, measuring at a point where the conductance has decreased by a decade means that the contacts will have at worst a 10% effect.

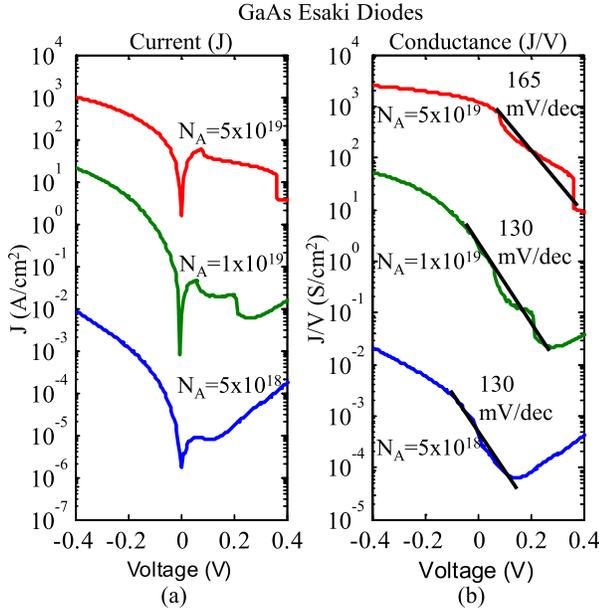


Fig. 5. (a) J versus V and (b) $G = J/V$ versus V for GaAs mesa diodes [8]. The diodes were grown by MBE at $N_D = 3 \times 10^{19}/\text{cm}^3$. The semilog conductance swing voltage = 130 mV/decade and then gets worse at heavier doping.

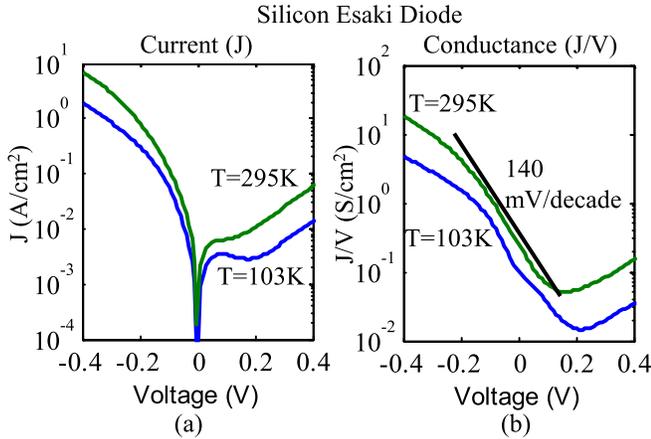


Fig. 6. (a) J versus V and (b) $G = J/V$ versus V for a silicon Esaki diode formed by implantation to about $n\text{-p} \sim 10^{20}/\text{cm}^3$ is plotted (sample PN-BF₂-Q8 in [14]). The semilog conductance swing voltage = 140 mV/decade regardless of the temperature. It appears to be limited by inhomogeneities and the presence of random dopant ions.

in swing accompanied by a large change in current indicates that the steepness cannot be a result of barrier thickness modulation. The barrier thickness modulation swing would have a strong dependence of current/tunneling probability as indicated in (6). The conductance smoothly passes through the origin of voltage, revealing the tunneling joint density of states, as predicted in (3). In the negative differential resistance regime, oscillations can occur during measurement that result in unrealistically sharp features. Consequently, in Fig. 5(b), we measure an average swing through the entire Esaki regime.

In Fig. 6, we show the current and conductance for a silicon Esaki diode formed by implantation to $\sim 1 \times 10^{20}/\text{cm}^3$ (sample PN-BF₂-Q8 in [14]). Here, we show the measurement at 295 and 103 K. Similar to Fig. 5, the semilog conductance swing voltage is 140 mV/decade.

In addition to analyzing Esaki diodes, we can also consider backward diodes that are tunneling diodes optimized to turn ON around zero bias. Backward diodes are usually specified by a figure of merit, the curvature coefficient γ , that can be used to estimate the semilog conductance swing voltage. γ is given by

$$\gamma \equiv \left. \frac{d^2 I / dV^2}{dI/dV} \right|_{V=0}. \quad (7)$$

To relate (7) to the semilog conductance swing voltage, we need a simple model for the current. From Fig. 2, $\mathcal{T} \times D_J(E)$ changes exponentially with bias and is therefore proportional to $\exp(-V/V_0)$, where V_0 is the exponential slope and gives the tunneling steepness. The negative sign is associated with backward diode action. Replacing $\mathcal{T} \times D_J(E)$ with $\exp(-V/V_0)$ in the current, (1), gives

$$I \propto \int (f_C - f_V) \times e^{-V/V_0} \times \partial E. \quad (8)$$

At small biases, we can Taylor expand the Fermi functions such that $f_C - f_V \propto V$ and so we get

$$I \propto V \times e^{-V/V_0}. \quad (9)$$

Plugging (9) into (7) gives

$$\gamma = -2/V_0 \quad (10)$$

V_0 can be converted to mV/decade to give $S_{\mathcal{T} \times D(E)}$: $S_{\mathcal{T} \times D(E)} = \ln(10) \times V_0$. Combining this with (10) gives

$$S_{\mathcal{T} \times D(E)} = \ln(10) \times V_0 = \ln(10) \times 2/\gamma. \quad (11)$$

To do better than 60 mV/decade the backward diode curvature coefficient should be $\gamma > 80$. This is twice the typical goal of $\gamma > 40$ for backward diodes. This can be seen from the fact that, we need to model the current as $I \propto V \times \exp(-V/V_0)$ rather than $I \propto \exp(-V/V_0) - 1$. The extra factor of V gives an extra factor 2 when taking the derivative.

The best backward diode curvature coefficient appears to be $\gamma = 47$ [15] and $\gamma = 50$ [16]. One paper claimed a $\gamma = 70$ [17], but did not show the I - V curve. In all cases, they fall short of a semilog conductance swing voltage steeper than 60 mV/decade.

In Fig. 7, a germanium backward diode with $\gamma = 50$ is shown. Using (11) to calculate the semilog conductance swing voltage gives 92 mV/decade, corresponding exactly to the measured value in Fig. 7(b).

In Fig. 8, we show an InAs/AlSb/Al_{0.12}Ga_{0.88}Sb heterojunction backward diode [15] with $\gamma = 47$ and a semilog conductance swing voltage of 98 mV/decade. In this diode, the tunneling barrier thickness is fixed by the AlSb thickness and so the conductance steepness is entirely due to the joint density of states. While various nonidealities or leakage currents may be limiting the device, this is the steepest turn ON that has been measured in the InAs/AlSb/AlGaSb system.

IV. ANALYZING TFETs

We can apply the same analysis that we have done so far to TFETs. In a TFET, we can either make a two terminal

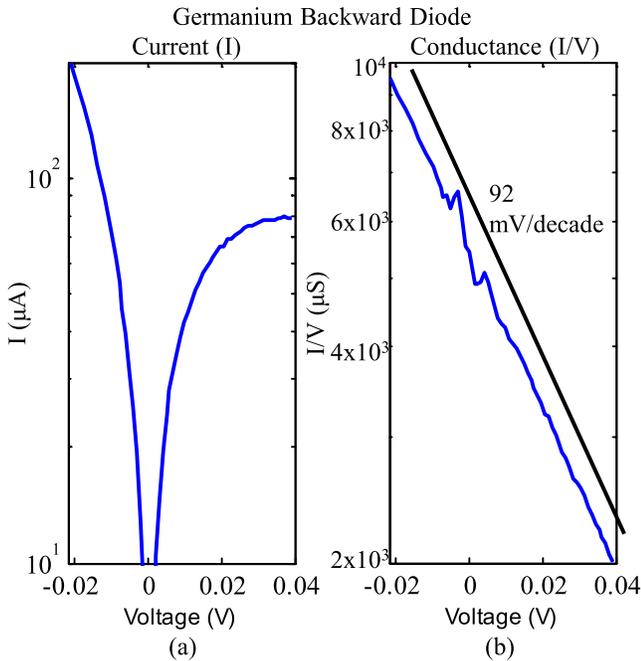


Fig. 7. (a) I versus V and (b) $G = I/V$ versus V for a germanium backward diode [16]. The semilog conductance swing voltage = 92 mV/decade is the steepest tunnel diode conductance swing voltage we could find in the literature for which an I - V curve was provided.

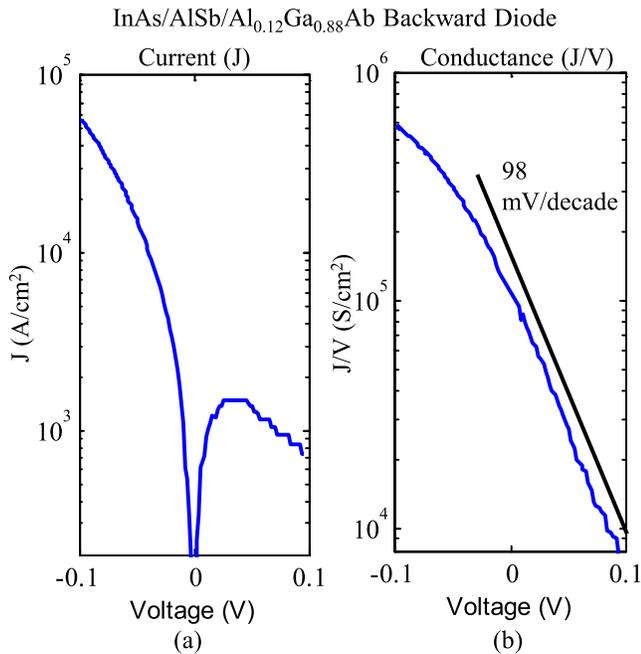


Fig. 8. (a) J versus V and (b) $G = I/V$ versus V for an InAs/AlSb/Al_{0.12}Ga_{0.88}As heterojunction backward diode [15]. This diode has one of the highest reported curvature coefficients, γ , and consequently lowest semilog conductance swing voltage reported in the literature. It also has one of the lowest doping levels of $1.4 \times 10^{17}/\text{cm}^3$ near the tunneling junction.

source-drain measurement, or a three terminal I_D - V_G measurement. In either case, the current is given by (1). In a three terminal measurement the Fermi occupation probability, $f_C - f_V$, is fixed by source-drain voltage, V_{DS} , while $\Gamma \times D_J(E)$ is changed by the applied gate bias. This means that measuring the subthreshold swing voltage will give the tunneling joint density of states. However, some voltage is

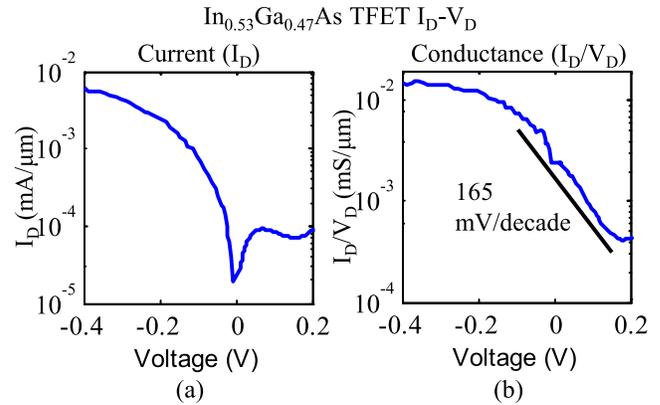


Fig. 9. (a) I_D versus V_D and (b) $G = I_D/V_D$ versus V_D for an In_{0.53}Ga_{0.47}As TFET [18]. The measured subthreshold swing voltage = 216 mV/decade while the semilog conductance swing voltage = 165 mV/decade. Since the I_D - V_D characteristic is not limited by the gate oxide, it reveals the junction's steeper intrinsic tunneling properties.

lost across the gate oxide and so the subthreshold swing voltage is increased by a poor gate efficiency.

If we want to avoid any gate issues, we can also do a two terminal measurement. If the critical tunneling junction is the source-channel junction, we need to fix the V_G - V_D voltage while measuring I_D - V_S . Since the gate potential will have a strong influence on the channel potential, the drain will not be able to effectively control the source-channel junction. On the other hand, if the critical tunneling junction is at the channel-drain junction, we want to measure I_D - V_D while fixing the V_G - V_S voltage.

In Fig. 9, we analyze the I_D - V_D characteristics of an In_{0.53}Ga_{0.47}As TFET at fixed V_G - V_S voltage. The measured subthreshold swing voltage is 216 mV/decade owing to the poor gate oxide [18]. The measured I_D - V_D semilog conductance swing voltage = 165 mV/decade. Since the I_D - V_D characteristic is not limited by the gate oxide deficiencies, it reveals the junction's steeper intrinsic tunneling properties.

This shows the value of using the semilog conductance swing voltage to analyze a TFET's potential performance when the gate oxide has poor quality.

In TFETs, subthreshold swing voltages <60 mV/decade have been measured, but only at extremely low-current densities of ~ 1 nA/ μm [19]–[23]. We now explain why this has not been observed in backward diodes and Esaki diodes. These diodes need heavy doping which moves the band overlap threshold to forward bias, where the low-current densities are obscured by leakage current. Consequently, the semilog conductance swing voltage can only be measured at higher current densities where it is not as steep. Contrariwise, in a transistor, the gate potential can ensure a narrow tunneling barrier with less doping and under reverse bias. 2-terminal measurements on a 3-terminal device are needed, with the gate acting only to adjust Fermi Levels. Furthermore, the diode electrostatics is not optimized for barrier thickness modulation, while the sub-60 TFET results are likely to be due to barrier thickness modulation [11], [12].

V. CONCLUSION

The absolute conductance, I/V , of either a tunneling diode or of a TFET source–drain I - V , is proportional to the tunneling joint density of states. This is true even as the applied voltage passes through zero. The joint-density-of-states behaves poorly, which will limit the prospective subthreshold swing voltage that we can expect from TFETs. This is likely due to the many nonidealities that smear the band edges. As a first step, doping which is inherently inhomogeneous, should be eliminated. Ultimately, a sharp threshold may even require structural reproducibility at the single atom level.

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REFERENCES

- [1] A. C. Seabaugh and Q. Zhang, “Low-voltage tunnel transistors for beyond CMOS logic,” *IEEE Proc.*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.
- [2] J. N. Schulman and D. H. Chow, “Sb-heterostructure interband backward diodes,” *IEEE Electron Device Lett.*, vol. 21, no. 7, pp. 353–355, Jul. 2000.
- [3] T. Tiedje, E. Yablonovitch, G. D. Cody, and B. G. Brooks, “Limiting efficiency of silicon solar cells,” *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 711–716, May 1984.
- [4] S. R. Johnson and T. Tiedje, “Temperature dependence of the urbach edge in GaAs,” *J. Appl. Phys.*, vol. 78, no. 9, pp. 5609–5613, 1995.
- [5] J. Knoch, S. Mantl, and J. Appenzeller, “Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices,” *Solid-State Electron.*, vol. 51, pp. 572–578, Apr. 2007.
- [6] M. A. Khayer and R. K. Lake, “Effects of band-tails on the subthreshold characteristics of nanowire band-to-band tunneling transistors,” *J. Appl. Phys.*, vol. 110, no. 7, p. 074508, 2011.
- [7] J. I. Pankove, “Absorption edge of impure gallium arsenide,” *Phys. Rev.*, vol. 140, pp. A2059–A2065, Mar. 1965.
- [8] D. Pawlik *et al.*, “Benchmarking and improving III-V esaki diode performance with a record 2.2 MA/cm² peak current density to enhance TFET drive current,” in *Proc. IEEE IEDM*, Dec. 2012, pp. 1–3.
- [9] S. Agarwal, J. T. Teherani, J. L. Hoyt, D. A. Antoniadis, and E. Yablonovitch, “Engineering the electron-hole bilayer tunneling field-effect transistor,” *IEEE Trans. Electron Devices*, 2014, doi: 10.1109/TED.2014.2312939.
- [10] E. O. Kane, “Theory of tunneling,” *J. Appl. Phys.*, vol. 32, no. 1, pp. 83–91, 1961.
- [11] S. Agarwal and E. Yablonovitch, “Designing a low voltage, high current tunneling transistor,” in *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits*, T.-J. K. Liu and K. Kuhn, Eds. Cambridge, U.K.: Cambridge Univ. Press, 2014.
- [12] S. Agarwal and E. Yablonovitch, “Fundamental tradeoff between conductance and subthreshold swing for barrier thickness modulation in tunneling field effect transistors,” Under Review.
- [13] M. Luisier and G. Klimeck, “Atomistic full-band design study of InAs band-to-band tunneling field-effect transistors,” *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 602–604, Jun. 2009.
- [14] P. M. Solomon *et al.*, “Universal tunneling behavior in technologically relevant P/N junction diodes,” *J. Appl. Phys.*, vol. 95, no. 10, pp. 5800–5812, 2004.
- [15] Z. Zhang, R. Rajavel, P. Deelman, and P. Fay, “Sub-micron area heterojunction backward diode millimeter-wave detectors with 0.18 pW/Hz^{1/2} noise equivalent power,” *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 5, pp. 267–269, May 2011.
- [16] J. Karlovsky and A. Marek, “On an Esaki diode having curvature coefficient greater than E/KT,” *Czechoslovak J. Phys.*, vol. 11, no. 1, pp. 76–78, 1961.
- [17] J. Karlovsky, “Curvature coefficient of germanium tunnel and backward diodes,” *Solid-State Electron.*, vol. 10, no. 11, pp. 1109–1111, 1967.
- [18] S. Mookerjee, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, “Temperature-dependent I-V characteristics of a vertical In_{0.53}Ga_{0.47}As tunnel FET,” *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010.
- [19] G. Dewey *et al.*, “Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep subthreshold swing,” in *Proc. IEEE IEDM*, Dec. 2011, pp. 1–4.
- [20] T. Krishnamohan, K. Donghyun, S. Raghunathan, and K. Saraswat, “Double-gate strained-ge heterostructure tunneling FET (TFET) with record high drive currents and < 60 mV/dec subthreshold slope,” in *Proc. IEEE IEDM*, San Francisco, CA, USA, Dec. 2008, pp. 1–3.
- [21] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, “Germanium-source tunnel field effect transistors with record high ION/IOFF,” in *Proc. Symp. VLSI Technol.*, Kyoto, Japan, 2009, pp. 178–179.
- [22] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, “Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,” *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.
- [23] K. Jeon *et al.*, “Si tunnel transistors with a novel silicided source and 46mV/dec swing,” in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2010, pp. 1–5.



Sapan Agarwal (M'06) received the B.S. degree in electrical engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, and the Ph.D. degree from the University of California, Berkeley (UC Berkeley), CA, USA, in 2007 and 2012, respectively.

He is currently a Post-Doctoral Fellow at UC Berkeley.



Eli Yablonovitch (F'92) received the Ph.D. degree in applied physics from Harvard University, Cambridge, MA, USA, in 1972.

He is a Professor of Electrical Engineering and Computer Sciences with the University of California, Berkeley, CA, USA, where he is the Director of the NSF Center for Energy Efficient Electronics Science.